Reconfigurable Interconnect

Lab 1

Adder

a) Full Adder: \[ a + b + C_{in} = 2C_{out} + S \]

b) 4-bit Adder: Put 4 Fadders in series a, b, a', b'

\[ a_0, b_0 \text{ etc are 1 bit each.} \]

Longest delay = \[ C_{in} \rightarrow C_1 \rightarrow C_2 \rightarrow C_3 \rightarrow C_{out} \]

Function (model delay) Simulation: Verify functionality

Post layout (delay): Verify clock cycles