I. (1) State diagram & state table

\[ \begin{array}{c|cc|c|cc} & N_S & \text{output} \\ \hline \text{Ps} & x=0 & x=1 \\ \hline S_0 & S_0 & S_1 & 1 & 0 \\ S_1 & S_0 & S_1 & 1 & 0 \\ \end{array} \]

(2-b) Design system with T-flip-flops & Mux. / J-K with NAND gate

\[ \begin{array}{c|c|c|c|c|c} X & Q_0 & N_{Q_0} & Q_0^+ & \text{output} & T_0 & J_0 \& K_0 \\ \hline 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 1 & 1 & 1 & 1 & 0 \\ 1 & 1 & 1 & 1 & 0 & 0 & 0 \\ \end{array} \]

2) \[ T_0 = \overline{X} \oplus Q_0 \]

\[ \begin{array}{c|c|c} Q_0 & 0 & 1 \\ \hline X & 0 & 1 \\ \hline \end{array} \]

3) \[ J_0 = X \]

\[ \begin{array}{c|c|c} J_0 & 0 & 1 \\ \hline K_0 & 0 & 1 \\ \hline \end{array} \]

\[ K_0 = X \]

\[ J_0 \quad K_0 \quad \text{JK ff} \]
Step1) Based on outputs

\[ P_1 = \begin{pmatrix} A \cdot G \cdot H \end{pmatrix} \begin{pmatrix} B \cdot D \cdot E \end{pmatrix} \begin{pmatrix} F \end{pmatrix} \]

\[ \begin{array}{c|c|c|c}
G_1 & G_2 & G_3 \\
\hline
A & 2 & 2 & 2 \\
b & 1 & 1 & 1 \\
c & 2 & 2 & 2 \\
\end{array} \]

Step2)

<table>
<thead>
<tr>
<th>G_1</th>
<th>G_2</th>
<th>G_3</th>
<th>G_4</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>B</td>
<td>D</td>
<td>E</td>
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<tr>
<td>C</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>H</td>
<td></td>
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</tbody>
</table>

Step3)

<table>
<thead>
<tr>
<th>G_1</th>
<th>G_2</th>
<th>G_3</th>
<th>G_4</th>
<th>G_5</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>B</td>
<td>D</td>
<td></td>
<td></td>
</tr>
<tr>
<td>C</td>
<td></td>
<td></td>
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<td></td>
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<td></td>
<td></td>
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<tr>
<td>H</td>
<td></td>
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</tbody>
</table>

Step4)

<table>
<thead>
<tr>
<th>G_1</th>
<th>G_2</th>
<th>G_3</th>
<th>G_4</th>
<th>G_5</th>
<th>G_6</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
</tr>
</tbody>
</table>

So, Final state \{A, \{c, G\}, \{B, D\}, \{E, F\}, \{H\}\}

2) To distinguish \(G_k, H\), we can choose any input \(a, b, c\), but when we chose \(a\), next state \(D, B\) are same group. We could not distinguish.

Since

So, we should choose \(b\). (Next state is \(A, C\)), but output is still same.

Step2) choose \(a\), \(E, B\) is not same group, but still same output

Step3) choose \(c\), \(E, H\) is different group, but same output

→ go to \(E, H\).

Step4) choose \(b\), \(E, B\) is different and output also different → (4)

Therefore, minimum length is 4 and output sequences are 0→1→2→...
\[ \text{\( a_q b_q \text{ Cout} \)} \]

\[ \text{\( \text{Cout} = a_q b_q + c_0 b_q + c_0 a_q \)} \]

\[ \text{\( S_4 = a_q' b_q' c_0 + a_q' b_q c_0' + a_q b_q c_0' + a_q b_q c_0 \)} \]

**From Same Method.**

\[ \text{\( a_q' \\ b_q' \\ c_0' \)} \]

\[ \text{\( a_q b_q c_0 \)} \]

\[ \text{\( \text{Converting} \)} \]

\[ \text{\( \text{Cout} \)} \]

\[ \text{\( \text{going into} \)} \]

\[ \text{\( \text{Cout} \)} \]
Consider the following schematic diagrams and information:

1. The first diagram illustrates a three-bit adder circuit with inputs and outputs labeled accordingly.
2. The second diagram shows a control circuit with inputs for $S_3$, $S_2$, $S_1$, and $S_0$, and outputs for the control signal $C_0$ and the clock $CLK$.
3. The text provides instructions for the operation of the control circuit.

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**Problem Statement:**

To find the LD input, determine the loading sequence for the given current number sequence.

**Current Number:**

1. $0000$  →  $1110$
2. $1011$  →  $0010$
3. $0011$  →  $1101$

**Loading Number:**

- $1110$
- $0010$
- $1101$

**Table:**

<table>
<thead>
<tr>
<th>Current No.</th>
<th>Loading No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>$0000$</td>
<td>$1110$</td>
</tr>
<tr>
<td>$1011$</td>
<td>$0010$</td>
</tr>
<tr>
<td>$0011$</td>
<td>$1101$</td>
</tr>
</tbody>
</table>

**LD Calculation:**

- For $S_3S_2S_1S_0 = 0000$, LD = 0
- For $S_3S_2S_1S_0 = 0010$, LD = 0
- For $S_3S_2S_1S_0 = 1101$, LD = 1

**Conclusion:**

- LD = $S_3/S_0$. If $S_3 = 0$, LD = 0; if $S_3 = 1$, LD = 1.
compare current \( N_0 \) & loading \( N_b \).

You can find \[ I_3 = I_{O} = S_3' \quad \& \quad I_2 = S_3 \oplus S_1 \]

\[
\begin{array}{c}
\text{0001} \\
\text{1011} \\
\text{0011} \\
\uparrow \uparrow \uparrow \uparrow \\
S_3, S_2, S_1, S_0
\end{array}
\]

\[
\begin{array}{c}
\text{1011} \\
\text{0010} \\
\uparrow \uparrow \uparrow \uparrow \\
I_9, I_8, I_7, I_6
\end{array}
\]

\[
\begin{array}{c}
I_1 = S_3 \oplus S_1
\end{array}
\]

\[
\begin{array}{c}
0 \quad 0 \quad 0 \quad 0 \\
1 \quad 1 \quad 0 \\
0 \quad 1 \quad 1
\end{array}
\]
<table>
<thead>
<tr>
<th>Operation</th>
<th>control signal</th>
<th>state</th>
</tr>
</thead>
<tbody>
<tr>
<td>Done=1</td>
<td>c1</td>
<td>s0</td>
</tr>
<tr>
<td>C=0</td>
<td>c2</td>
<td>s0</td>
</tr>
<tr>
<td>Done=0</td>
<td>c3</td>
<td>s1</td>
</tr>
<tr>
<td>A=0</td>
<td>c4</td>
<td>s1</td>
</tr>
<tr>
<td>B=Y</td>
<td>c5</td>
<td>s1</td>
</tr>
<tr>
<td>Z=0</td>
<td>c6</td>
<td>s1</td>
</tr>
<tr>
<td>C=INC(C)</td>
<td>c7</td>
<td>s1</td>
</tr>
<tr>
<td>B=ADD(A,B)</td>
<td>c8</td>
<td>s2</td>
</tr>
<tr>
<td>Z=INC(Z)</td>
<td>c9</td>
<td>s4</td>
</tr>
<tr>
<td>C=ADD(C,C)=SHL(C)</td>
<td>c10</td>
<td>s5</td>
</tr>
</tbody>
</table>

s3: If B goto pass  
s6: If C goto wait else goto loop  

a)