Lecture 2
Fault Modeling

- Why model faults?
- Some real defects in VLSI and PCB
- Common fault models
- Stuck-at faults
  - Single stuck-at faults
  - Fault equivalence
  - Fault dominance and checkpoint theorem
  - Classes of stuck-at faults and multiple faults
- Transistor faults
- Summary
Why Model Faults?

- I/O function tests inadequate for manufacturing (functionality versus component and interconnect testing)
- Real defects (often mechanical) too numerous and often not analyzable
- A fault model identifies targets for testing
- A fault model makes analysis possible
- Effectiveness measurable by experiments
Some Real Defects in Chips

- Processing defects
  - Missing contact windows
  - Parasitic transistors
  - Oxide breakdown
  - ...

- Material defects
  - Bulk defects (cracks, crystal imperfections)
  - Surface impurities (ion migration)
  - ...

- Time-dependent failures
  - Dielectric breakdown
  - Electromigration
  - ...

- Packaging failures
  - Contact degradation
  - Seal leaks
  - ...

# Observed PCB Defects

<table>
<thead>
<tr>
<th>Defect classes</th>
<th>Occurrence frequency (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Shorts</td>
<td>51</td>
</tr>
<tr>
<td>Opens</td>
<td>1</td>
</tr>
<tr>
<td>Missing components</td>
<td>6</td>
</tr>
<tr>
<td>Wrong components</td>
<td>13</td>
</tr>
<tr>
<td>Reversed components</td>
<td>6</td>
</tr>
<tr>
<td>Bent leads</td>
<td>8</td>
</tr>
<tr>
<td>Analog specifications</td>
<td>5</td>
</tr>
<tr>
<td>Digital logic</td>
<td>5</td>
</tr>
<tr>
<td>Performance (timing)</td>
<td>5</td>
</tr>
</tbody>
</table>

Common Fault Models

- Single stuck-at faults
- Transistor open and short faults
- Memory faults
- PLA faults (stuck-at, cross-point, bridging)
- Functional faults (processors)
- Delay faults (transition, path)
- Analog faults
Fault Model Types

- Levels
  - Behavioral (instruction, branch, ...)
  - RTL
  - Gate (stuck-at, structural, logical, ...)
  - Transistor (defect-oriented, stuck-open, stuck-short, pin)

- Domain
  - Microprocessor (assertion, branch, instruction, ...)
  - PLA (crosspoint, shrinkage, growth, (dis)appearance)
  - Memory (pattern sensitive)

- Fault Behavior (hyperactive, initialization, multiple, redundant, intermittent/permanent, parametric, race, potentially detectable, untestable, ...)

- Manifestation
  - Delay (line, gate, path, segment, transition)
  - Current (iddQ)
  - Bridging
Three properties define a single stuck-at fault:

- Only one line is faulty
- The faulty line is permanently set to 0 or 1
- The fault can be at an input or output of a gate

Example: XOR circuit has 12 fault sites (●) and 24 single stuck-at faults.

Test vector for h s-a-0 fault: &

Faulty circuit value

Good circuit value
Fault Equivalence

- Number of fault sites in a Boolean gate circuit is
  \[ = \#PI + \#\text{gates} + \# \text{ (fanout branches)} \]
- Fault equivalence: Two faults \( f_1 \) and \( f_2 \) are equivalent if all tests that detect \( f_1 \) also detect \( f_2 \) AND vice versa.
- If faults \( f_1 \) and \( f_2 \) are equivalent then the corresponding faulty functions are identical.
- Fault collapsing: All single faults of a logic circuit can be divided into disjoint equivalence subsets, where all faults in a subset are mutually equivalent. A collapsed fault set contains one fault from each equivalence subset.
Equivalence Rules

- **AND**
- **NAND**
- **OR**
- **NOR**
- **WIRE**
- **NOT**
- **FANOUT**
Equivalence Example

Faults in boldface removed by equivalence collapsing

Collapse ratio $= \frac{20}{32} = 0.625$
Fault Dominance

- If all tests of some fault $F_1$ detect another fault $F_2$, then $F_2$ is said to dominate $F_1$.
- Dominance fault collapsing: If fault $F_2$ dominates $F_1$, then $F_2$ is removed from the fault list.
- When dominance fault collapsing is used, it is sufficient to consider only the input faults of Boolean gates.
- In a tree circuit (without fanouts) PI faults form a dominance collapsed fault set.
- If two faults dominate each other then they are equivalent.
Dominance Example

A dominance collapsed fault set
Dominance Example

Faults in red removed by equivalence collapsing

Faults in yellow removed by dominance collapsing

Collapse ratio $= \frac{15}{32} = 0.47$
Checkpoints

Primary inputs and fanout branches of a combinational circuit are called \textit{checkpoints}.

Checkpoint theorem: A test set that detects all single (multiple) stuck-at faults on all checkpoints of a combinational circuit, also detects all single (multiple) stuck-at faults in that circuit.

Total fault sites = 16

Checkpoints (\red{\textbullet}) = 10
Classes of Stuck-at Faults

- Following classes of single stuck-at faults are identified by fault simulators:
  - **Potentially-detectable fault** -- Test produces an unknown (X) state at primary output (PO); detection is probabilistic, usually with 50% probability.
  - **Initialization fault** -- Fault prevents initialization of the faulty circuit; can be detected as a potentially-detectable fault.
  - **Hyperactive fault** -- Fault induces much internal signal activity without reaching PO.
  - **Redundant fault** -- No test exists for the fault.
  - **Untestable fault** -- Test generator is unable to find a test.
Multiple Stuck-at Faults

- A multiple stuck-at fault means that any set of lines is stuck-at some combination of (0,1) values.
- The total number of single and multiple stuck-at faults in a circuit with $k$ single fault sites is $3^k - 1$.
- A single fault test can fail to detect the target fault if another fault is also present, however, such masking of one fault by another is rare.
- Statistically, single fault tests cover a very large number of multiple faults.
Transistor (Switch) Faults

- MOS transistor is considered an ideal switch and two types of faults are modeled:
  - Stuck-open -- a single transistor is permanently stuck in the open state.
  - Stuck-short -- a single transistor is permanently shorted irrespective of its gate voltage.

- Detection of a stuck-open fault requires two vectors.
- Detection of a stuck-short fault requires the measurement of quiescent current ($I_{DDQ}$).
Stuck-Open Example

Vector 1: test for A s-a-0 (Initialization vector)
Vector 2 (test for A s-a-1)

Two-vector s-op test can be constructed by ordering two s-at tests

Stuck-open

Good circuit states

Faulty circuit states

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**Stuck-Short Example**

Stuck-short example with a circuit diagram showing the difference between good and faulty circuit states.

- **Good circuit state**: Test vector for $A = \text{a-0}$.
- **Faulty circuit state**: $I_{DDQ}$ path in faulty circuit.

Diagram features:
- pMOS FETs
- nMOS FETs
- $V_{DD}$
- $I_{DDQ}$ path
- Good circuit state (0)
- Faulty circuit state (X)
Summary

- Fault models are analyzable approximations of defects and are essential for a test methodology.
- For digital logic single stuck-at fault model offers best advantage of tools and experience.
- Many other faults (bridging, stuck-open and multiple stuck-at) are largely covered by stuck-at fault tests.
- Stuck-short and delay faults and technology-dependent faults require special tests.
- Memory and analog circuits need other specialized fault models and tests.