CSE 243A (Section Id: 947925)  
VLSI Computer-Aided Design  
Synthesis Methodologies in VLSI Design & Test  

Conference Reading List  

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  – What are the similarities in the CNN models that the paper explored?
  – CNNs have been successful in capturing spatial features of images. The paper illustrates one possible approach to map DFG into an image as shown in Figure 6. What do you think are some strengths and shortcomings of the proposed mapping?

  
  – The paper solves the optimization problem by traversing the graph and greedily evaluates decision variables in a breadth-first manner in order of dependencies. Why does it choose this specific order?

  
  – In what situations will the proposed soft error detection framework yield an LUT overhead similar to that resulted from DMR? Please explain.

• Matthew M. Ziegler, George Gristede and Victor V. Zyuban. “Power reduction by aggressive synthesis design space exploration” International Symposium on Low Power Electronics and Design (ISLPED), Beijing, China, September 2013, pp. 421–426. Darren; Nov. 28, 5:00 PM
  
  – Ideally, the proposed exploration would investigate all parallel design points within a job step. What are some scenarios where a certain parallel design point is immediately withdrawn from consideration, or the creation of its derivative blast zone may be aborted?

Suppose that the Reed-Solomon decoder shown in Figure 2 is to be instantiated with 4-bit LUTs without considering pipelining. What is the optimal number of LUTs? Please provide some justifications for your answer.

Please summarize how the proposed MILP formulations handle the constraints related to pipelining.


What are the metrics used to guide the optimization in resource sharing and binding? Why are they good metrics?

Section IV presents two atomic functions $\text{sum}(A, B)$ and $\text{max}(A, B)$. In what situations will we apply each function in the statistical timing analysis?


How does the proposed flexible memory controller allow the reuse of the same physical banks to store different data structures?

Please explain how the memory compatibility graph is constructed, and how to obtain the minimum number of parallel banks (M) from it.

Xitong Gao, John Wickerson and George A. Constantinides. “Automatically Optimizing the Latency, Area, and Accuracy of C Programs for High-Level Synthesis” *Proceedings of the 2016 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays*, Monterey, CA, USA, February 2016, 234–243. Yiyu; Nov. 28, 6:00 PM

The minimum latency transformation of Figure 1 is presented in the middle of page 3. Suppose that each operation is of unit delay. What is one possible execution order of instructions inside the loop? What is the minimum initiation interval ($I_{\text{min}}$) and the latency of the pipeline?

Comparing with SOAP2, what is the novelty of SOAP3 in its algorithm and transformation rules? Why are they introduced?