Successful Entrepreneurship for Microsystems

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Course presented at UCSD CSE 190, Fall Quarter 2015
Smartphones drive diverse technologies

- User Experience
- Performance
- Compact
- Low Cost
- Battery Life
- Low Power
- Architecture, SW, Design, ...
- More Moore
- More than Moore

- FC + WB stack
- TSV + FC stack
- TSV system stack
- MEMS Sensors

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Semiconductor Industry Evolution...“More Moore”

...Transistor complexities have doubled every 2 years

Source: IC Knowledge, ISSCC, TCX

Moore’s Law
2x / 12mos...1965-70
2x / 18mos...1970-90’s
2x / 24mos...now

+43% / year

-13% / year

Fabless Co.’s

Semiconductor Co’s – Fairchild, T.I., Motorola, National, Intel, Toshiba, …

System Co.’s – IBM, Hitachi, Sony, Philips, Unisys,…

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Moore's Scaling...is "forever delay" at the limit?

Ref: IMEC ITF July 2012
ECONOMIC challenges are threatening increased cost of capital, R&D, and design. Costs associated with node progression have been rising significantly.

<table>
<thead>
<tr>
<th>Fab cost</th>
<th>Process development cost</th>
<th>Chip design cost including fabless overhead costs*</th>
</tr>
</thead>
<tbody>
<tr>
<td>$ Millions</td>
<td>$ Millions</td>
<td>$ Millions</td>
</tr>
<tr>
<td>130nm</td>
<td>90nm</td>
<td>65nm</td>
</tr>
<tr>
<td>1,450</td>
<td>1,800</td>
<td>2,500</td>
</tr>
<tr>
<td>&gt;30%</td>
<td>~40%</td>
<td>~60%</td>
</tr>
</tbody>
</table>

* Chip design cost includes product R&D cost (design, verification & photomask) and other fabless costs (overhead, IP licensing, etc.)
Worldwide Growth of Fabless Companies

Number of Fabless Companies Worldwide by Year

Source: Global Semiconductor Alliance (formerly FSA)

Fabless Industry pioneered by innovators with ideas, but without wafer fabs

Consolidation
Reduced Venture Funding
### Top 10 Semiconductor Sales Leaders

<table>
<thead>
<tr>
<th>Rank</th>
<th>2013 Rank</th>
<th>2012 Rank</th>
<th>Company</th>
<th>HQ</th>
<th>2013 Revenue ($M)</th>
<th>2013/2012 Change</th>
<th>Market Share</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>Intel Corporation</td>
<td>U.S.</td>
<td>$46,960</td>
<td>-1%</td>
<td>14.8%</td>
</tr>
<tr>
<td>2</td>
<td>2</td>
<td>2</td>
<td>Samsung Electronics Co., Ltd</td>
<td>South Korea</td>
<td>$33,456</td>
<td>+7%</td>
<td>10.5%</td>
</tr>
<tr>
<td>3</td>
<td>3</td>
<td>6</td>
<td>QUALCOMM - QCT Division</td>
<td>U.S.</td>
<td>$17,341</td>
<td>+31.6%</td>
<td>5.5%</td>
</tr>
<tr>
<td>4</td>
<td>10</td>
<td>9</td>
<td>Micron Technology, Inc.</td>
<td>U.S.</td>
<td>$14,168</td>
<td>+109%</td>
<td>4.5%</td>
</tr>
<tr>
<td>5</td>
<td>7</td>
<td>8</td>
<td>SK Hynix</td>
<td>South Korea</td>
<td>$13,335</td>
<td>+48.7%</td>
<td>4.2%</td>
</tr>
<tr>
<td>6</td>
<td>5</td>
<td>4</td>
<td>Toshiba Semiconductor Co.</td>
<td>Japan</td>
<td>$12,459</td>
<td>+11.9%</td>
<td>3.9%</td>
</tr>
<tr>
<td>7</td>
<td>4</td>
<td>3</td>
<td>Texas Instruments</td>
<td>U.S.</td>
<td>$11,379</td>
<td>-5.5%</td>
<td>3.6%</td>
</tr>
<tr>
<td>8</td>
<td>9</td>
<td>10</td>
<td>Broadcom</td>
<td>U.S.</td>
<td>$8,121</td>
<td>+3.5%</td>
<td>2.6%</td>
</tr>
<tr>
<td>9</td>
<td>8</td>
<td>7</td>
<td>STMicroelectronics</td>
<td>Europe</td>
<td>$8,076</td>
<td>-4.9%</td>
<td>2.9%</td>
</tr>
<tr>
<td>10</td>
<td>6</td>
<td>5</td>
<td>Renesas Electronics</td>
<td>Japan</td>
<td>$7,822</td>
<td>-15.3%</td>
<td>2.5%</td>
</tr>
</tbody>
</table>

Source: IHS iSuppli, Wiki, March 2014
# Fabless Companies in Top 20 Semiconductor Revenue

<table>
<thead>
<tr>
<th>2013 Rank in Top 20</th>
<th>2012 Rank in Top 20</th>
<th>Company</th>
<th>Headquarters</th>
<th>2013 Revenue ($M)</th>
<th>2013/2012 Rev. Change ($M)</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>3</td>
<td>Qualcomm</td>
<td>U.S.</td>
<td>17,341</td>
<td>+31.6%</td>
</tr>
<tr>
<td>8</td>
<td>9</td>
<td>Broadcom</td>
<td>U.S.</td>
<td>8,121</td>
<td>+3.5%</td>
</tr>
<tr>
<td>12</td>
<td>12</td>
<td>AMD</td>
<td>U.S.</td>
<td>5,076</td>
<td>-4.2%</td>
</tr>
<tr>
<td>14</td>
<td>18</td>
<td>MediaTek</td>
<td>Taiwan</td>
<td>4,434</td>
<td>+32.1%</td>
</tr>
<tr>
<td>17</td>
<td>15</td>
<td>Nvidia</td>
<td>U.S.</td>
<td>3,612</td>
<td>-5.6%</td>
</tr>
<tr>
<td>18</td>
<td>19</td>
<td>Marvell</td>
<td>U.S.</td>
<td>3,281</td>
<td>+3.6%</td>
</tr>
<tr>
<td>20</td>
<td>23</td>
<td>Analog Devices</td>
<td>U.S.</td>
<td>2,677</td>
<td>+0.2%</td>
</tr>
</tbody>
</table>

*Others: SanDisk, Avago, Xilinx, Altera, LSI Logic*

Source: IHS iSuppli, Wiki, March 2014
Fabless Eco-system Alignment Across Entire Value Chain is Required
The “Productization / Commercialization” Lifecycle
…Idea to High Volume Production

Technology Release Levels, Ref. nasa.gov

1 2 4 5 7 9
The “Productization / Commercialization” Lifecycle
...Idea to High Volume Production

- Idea
- Lab Demo: Funding, Market, Customer, Biz Plan...
- Model Prototype: “System”/Produce-able Prototype
- Production

Technology Release Levels, Ref. nasa.gov
1 2 4 5 7 9

- Understand Problem
- Define Solution
- Validate Qualitatively
- Verify Quantitatively

- Problem/Solution Fit
- Product/Market Fit

- CANVAS
- Customer Discovery
- Customer Interviews
- 1st Demo/Sample

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The HCD process...solve the RIGHT PROBLEM
- Meet people’s NEEDS
- Product is UNDERSTANDABLE and USABLE, ACCOMPLISHES the expected TASKS
- User's EXPERIENCE is positive and enjoyable

The Design process
- OBSERVE
- GENERATE IDEAS (Ideation)
- PROTOTYPE
- TEST

Ref.: Don Norman, “The Design of Everyday Things”, Chapter 6
Human Centered Design
…UCSD Design Lab…Prof. Don Norman

Figure 6.1. The Double-Diamond Model of Design.

Ref.: Don Norman, “The Design of Everyday Things”, Chapter 6
Product Development Lifecycle

- Internal Development at big Company
- Idea / MVP
- Software Product
- License IP
- OEM* Product
- Fabless I.C. company

Existing
- Standard, Technology
- Market
- Customer Base

New
## Success elements – product positioning

<table>
<thead>
<tr>
<th>EXISTING</th>
<th>NEW</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standard, market, customer base</td>
<td>Standard, market, customer base</td>
</tr>
<tr>
<td>➢ Super-Integration</td>
<td>➢ Emerging standard</td>
</tr>
<tr>
<td>➢ Problem solutions</td>
<td>➢ New features/capabilities</td>
</tr>
<tr>
<td>➢ Evolutionary enhancements</td>
<td>➢ New interfaces</td>
</tr>
<tr>
<td>➢ e.g. Cost reduction</td>
<td>➢ “Revolutionary” enhancements</td>
</tr>
</tbody>
</table>

Will Impact Schedule, Technology Selection, Design Methodology,....
Conceptual timeline

Existing markets:

<table>
<thead>
<tr>
<th>Chip Development</th>
<th>Market Accept</th>
<th>Ramp</th>
<th>Hi Volume</th>
</tr>
</thead>
</table>

~5 quarters

For existing markets, getting the product to market and increasing market share is important!

New markets:

<table>
<thead>
<tr>
<th>Chip Development</th>
<th>1st Customer</th>
<th>Slow Ramp</th>
<th>Hi Volume</th>
</tr>
</thead>
<tbody>
<tr>
<td>Alliance / New Standard Accept</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Key: early engagement with customer to evaluate and validate the new chip.

J. Fiebiger (Board Directors Actel, Mentor, QLogic):

“The fabless company must identify the first potential customer early. It is important to have customer’s input in shaping the product requirements… Investors and suppliers will get a favorable story when they perform due diligence with the customer about the viability of the product and potential volume.”
Lifecycle of a Fabless IC development – the 4 phases

- Global Planning
- IC Design
- IC Prototyping
- IC Production

Series A

Series B

30 – 50% of TT$
Lifecycle of a Fabless IC development – activity highlights

“System” Architecture / Design / Simulation / Verification

FPGA Implementation
Reference Design
Customer Evaluation “Proof of Concept”

Customer Samples
Reference Boards
Customer Evaluation Design Acceptance

Global Planning
High Level Design
Floor Planning

IC Design
Chip Design
RTL
NL

Physical Design
NL
GDSII

Analog IP Design

IC Prototyping
IC Production
IC Qualification
Prod. Ramp
Debug
Hi volume

Series A
Series B

30 – 50% of TT$
Typical ASIC Development Cycle

Start Design

ASIC DESIGN

FPGA
Proto
Ref Board
Tapeout
ES
QS
Prod
HW/SW
Launch

Year 0
Year 1
Year 2

Software
α
Software
β
Software
Prod.

Initial Silicon
Initial Silicon Ramp
Initial Product Ramp
Volume Production

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System vs. IC Development Cycle

a. At the System company:

Start Product Design

- Year 0
- Year 1
- Year 2

Launch

b. At the Fabless IC company:

- Start Design
- Tapeout
- ES
- QS
- Prod HW/SW
- Launch

Volume Orders

- Year 0
- Year 1
- Year 2
Typical Software Development Cycle

Year 1
- Requirements Spec.
- Design & Development
- Integration
- Testing & Debug
- Preview Release/Public β Release
- Final Release
- Iterations/Additional Releases

Year 2
- α
- β
- Δ
HW 7 – Lean Canvas

...Due Thursday, 5th

➤ Describe an approximate Timeline/Lifecycle for your team’s Product
In-class Quiz 6-2

List the 3 most important learnings from today’s lecture