Quiz #6 A

No books, no notes
no electronics except for clicker
Question #1: 2 min

What is delay of the (longest path, shortest path) given AND_delay=10ps & OR_delay=15ps?

A. (40ps, 10ps)
B. (25ps, 10ps)
C. (25ps, 15ps)
D. (40ps, 15ps)
E. None of the above
What is true about the load and clear signals of local register “Creg” when converting this HLSM to FSM?

A. load=1 only in inc and dec states
B. load=1 only in inc, dec and init states
C. clear=1 only in init state
D. A and C
E. None of the above
Based on the given HLSM, under what circumstances is the register “reg” incremented?

A. go=1, C=1, B=1  ✔️
B. go=1, C=0, B=1  ❌
C. go=1, C=0, B=0  ❌
D. A and B  ❌
E. A and C  ✔️
Question #4 3 min

In the circuit shown below, D-FFs have max/min delay for output of 5ps/2ps respectively, Thold=1ps, and Tsetup=5ps. Logic gates have max/min delay of 10ps/5ps respectively. Clock period is 20ps, and it deviates from the nominal arrival time by as much as 5ps. Which statement is true for this circuit:

A. Hold time is violated, need to add a buffer
B. Hold time is violated, need to change clk period
C. Setup time is violated, need to increase clk period
D. Setup time is violated, need to decrease clk period
E. None of the above
Question #5: 4 min

HLSM is currently in state S2. What is Dreg value for the provided L & S, after 9 clock cycles?

A. 6
B. 3
C. 0
D. 9
E. None of the above