Quiz #4

No books, no notes
no electronics except for clicker
Question #1: 1min

Following are the properties of an S-R latch:

A. Sets output $Q=1$ when $S=1$, $R=0$
B. Resets output $Q=0$ when $S=0$, $R=1$
C. Acts as memory by holding prev $Q$ when $S=0$, $R=0$
D. All of the above
E. None of the above
Question #2: 2min

D latch is built by adding blocks P, Q, R to an SR latch. What gates do they represent?

A. NOR, NOR, INV
B. AND, OR, INV
C. AND, AND, INV
D. OR, AND, INV
E. None of the above
Question #3: 3min

This ALU bit slice satisfies the following:

A. If f[2:0]=111, then $S_i=a_i + b_i$
B. If f[2:0]=011, then $S_i=a_i - b_i$
C. If f[2:0]=100, then $S_i=a_i \oplus b_i'$
D. Two or more of the above
E. None of the above
Question #4: 4min

Adjacent diagram represents a type of latch with A and B inputs. What are the values of p, q r in the truth table below?

<table>
<thead>
<tr>
<th></th>
<th>A</th>
<th>B</th>
<th>Q</th>
</tr>
</thead>
<tbody>
<tr>
<td>p</td>
<td>1</td>
<td>0</td>
<td>p</td>
</tr>
<tr>
<td>q</td>
<td>0</td>
<td>1</td>
<td>q</td>
</tr>
<tr>
<td>r</td>
<td>0</td>
<td>0</td>
<td>r</td>
</tr>
</tbody>
</table>

A. p=1, q=0, r=0
B. p=0, q=1, r=1
C. p=1, q=1, r=0
D. p=0, q=0, r=1
E. None of the above
Question #5: 4min

Positive edge triggered D-FF and level high sensitive D-latch both have CL (clock) and D_in as inputs. Find which waveform (Q1, Q2, Q3) represents the output of the D-FF, and which is for D-latch.

A. D-FF: Q2, D-latch: Q3
B. D-FF: Q3, D-latch: Q2
C. D-FF: Q1, D-latch: Q2
D. D-FF: Q2, D-latch: Q1
E. None of the above