CSE140: Bonus Take-Home Final Questions

Due to tajana@ucsd.edu via email on Friday, 12/11, 5pm (put CSE140 bonus final in subject)

Maximum 1% bonus to your final grade

Note: This is an individual assignment; do not discuss this with anybody from class.

If I have a reason to suspect you of cheating, you can get an F in the class.

Inputs: byte a[256], byte b[256], bit go
Outputs byte a_gt_b, a_eq_b, a_lt_b, bit done

while (1) {
    while (!go);
    done := 0;
    i:=0;
    a_lt_b :=0;
    a_gt_b := 0;
    a_eq_b :=0;
    while ( i < 256 ) {
        if ( a[i] < b[i] ) a_lt_b := a_lt_b + 1;
        else if ( a[i] == b[i] ) a_eq_b := a_eq_b + 1;
        else a_gt_b := a_gt_b + 1;
        i := i + 1;
    }
    done := 1;
}

1. Convert C code provided above into a high-level finite state machine.
2. Create the datapath for this design, show all connections and components.
3. Connect the datapath to the controller, label all signals.
4. Design the controller FSM. Create a state table showing inputs, current/next state, and outputs.
5. Use binary encoding to encode the states and provide the excitation table.
6. Implement the controller using D-FFs and the excitation table you provided.
7. Show a gate level design of each element in your datapath. Use D-FF where needed.
8. What is the critical path in your design?
   Assume each gate’s delay = 1ns * #gate_inputs. For example, an inverter’s delay is 1ns, while three input NOR gate has 3ns delay. Pass gate has the same delay as an inverter.
   Quantify the delay of the critical path.
9. Optimize your design to have minimum TRANSISTOR count. Draw the new implementation; for repetitive blocks show the transistor level design of only one of the elements (e.g. if you have 8 D-FFs, show transistor implementation of only one of them).
10. Calculate the maximum clock frequency of your design. For all D-FFs use setup time/hold time of 2ns and clock skew of 3ns. Justify your answer.
11. Now assume that array of 256 8-bit values is stored in DRAM. Show how you’d design a special purpose DRAM chip for this problem. Draw all components needed for the data access to work. Show timing diagrams illustrating how to store and fetch 8-bit data to/from DRAM. How many transistors total for your design including the DRAM chip?
12. Assume that the time for any type of data transfer between the rest of your design and DRAM is 50 clock cycles (the clock cycle time you calculated earlier). Given this, estimate how long will your design take to get the final result?
13. What dominates the performance and area of your designs?
   Estimate area by counting transistors.