1. a. HLSM:

Inputs: go (bit), a (256-byte memory), b (8 bits)
Outputs: done (bit), freq (8 bits)

b. Data path:
c. control path FSM:

Inputs: go, i_lt_256, a_eq_b (bit)
Outputs: done, i_clr, i_ld, freq_clr, freq_ld (bit)

---

d. connection between control path and the data path:
2.

a. HLSM:

Inputs: U (bit), D (bit)
Outputs: C (16 bits)
Local registers: Creg (16 bits)

b. Datapath:
c. Control FSM:

\[ (UD'v' + U'Dv')' \]

\[ UD'v' \]

\[ (U'Dv)' \]

\[ U'Dv' \]

\[ \text{Init} \quad \text{clr} = 1 \quad \text{ld} = 0 \]

\[ \text{Wait} \]

\[ \text{PressU} \quad \text{ld} = 1 \]

\[ \text{WaitRelU} \quad \text{ld} = 0 \]

\[ \text{PressD} \quad \text{ld} = 1 \]

\[ \text{WaitRelD} \quad \text{ld} = 0 \]

\[ D' \]

\[ D \]

v is the output from the datapath.

\[ v = 1 \text{ when } D = 0 \text{ and } C_{\text{reg}} = 65535 \]

\[ v = 1 \text{ when } D = 1 \text{ and } C_{\text{reg}} = 0 \]

d. Connections:
3.

a. HLSM:

b. FSM:
clr = D1’ D0’ = D1 nor D0
ld = D1D0’

D1 = B

<table>
<thead>
<tr>
<th>B\D1D0</th>
<th>00</th>
<th>01</th>
<th>11</th>
<th>10</th>
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<tr>
<td>1</td>
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D0 = B’ + D1 + D0

<table>
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<tr>
<th>B\D1D0</th>
<th>00</th>
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c. controller:

![Controller Diagram]

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d. datapath and connections:

![Datapath Diagram]
4.

a. High Level FSM

*Inputs:* 1 (32 bits), b (bit), c (bit), d (bit)
*Outputs:* 1 (32 bits)
*Local registers:* offset (32 bits), Jreg (32 bits)
b) Data Path:

All data transfer lines, I and J are 32 bit, all inputs to the Datapath block are single bit.
When ld = 0, the register holds its value
    ld = 1, the register loads the value fed to it

Other correct implementations of the datapath should be given full marks

c) Control FSM

If any output values are missing, assume 0.
d) Connections from Controller to DataPath