1. Design a 4-bit Arithmetic Unit (AU) with the following functional table:

<table>
<thead>
<tr>
<th>$M_1$</th>
<th>$M_0$</th>
<th>Function Name</th>
<th>$F(A,B)$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>$A + A$ multiplied by 8 times $B$</td>
<td>$A \times (8 \times B) + A$</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>If $(A&gt;B)$ subtract $B$ from $A$; otherwise add $A$ and $B$</td>
<td>If $(A&gt;B)$ then $A - B$; else $A + B$</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Decrement $A$</td>
<td>$A - 1$</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Add 1 to $A + B$</td>
<td>$A + B + 1$</td>
</tr>
</tbody>
</table>

where $A$ and $B$ are two 4-bit binary numbers $a_3a_2a_1a_0$ and $b_3b_2b_1b_0$.

$M_1$, $M_0$ are the control inputs to this AU.

Design this 4-bit AU using only the minimum number of Full Adders, Comparators and Multiplexers.

2. Design a circuit that finds an 8-bit input value ‘X’ inside a $1024 \times 8$ memory and returns its address when found; if not found return -1. The circuit begins when a ‘START’ signal is set to 1 and asserts a ‘DONE’ signal at completion.

A. Design a high-level state machine

B. Create the datapath using minimum number of the following components RAM, Adder, Comparator, and Register

C. Connect the datapath to controller

3. A 4-bit ring counter counts according to the sequence $1000 \rightarrow 0100 \rightarrow 0010 \rightarrow 0001 \rightarrow 1000$ and repeats. A reset input places the counter into state 1000. Design this circuit using the following pre-designed components:

- A 2-to-4 decoder;
- A pre-designed, positive edge-triggered, 2-bit up-counter that counts as $00 \rightarrow 01 \rightarrow 10 \rightarrow 11 \rightarrow 00$ and repeats. In addition to the clock trigger input, this counter has a reset input which can be used to reset it to 00.
- A minimum number of AND/OR/NOT gates (only if needed).
4. A recognizer has a single input X and two outputs (Z1 and Z2). The output Z1 becomes 1 each time the input sequence 101 is observed. Otherwise Z1=0. The output Z2=1 each time input sequence 011 is observed, otherwise Z2=0. For example, for the input X={10101101}, the outputs are: Z1={00101001}, and Z2={00000100}.

A. Draw the Mealy style state diagram of this machine

B. Implement the FSM using a shift register and a minimum number of gates.