1. A serial subtractor has two inputs X and Y of N bits each. The subtractor takes two bits \( x_i \) and \( y_i \) and generates a single output \( d_i \) (the difference) for each clock cycle. Design a Mealy FSM for the \( i^{th} \) bit of this subtractor.

   a. Draw the state diagram.
   b. Write the state table (Present state, Inputs, Next state, Output).
   c. Derive the equations for Next state and Output.
   d. Realize the FSM using D-flip flops.

   Hint: Think about how subtraction operation uses borrow to perform subtraction in binary and leverage that to define the states.

2. For the circuit shown in Fig. 1:

   a. Calculate the maximum clock frequency for operation. (Assume that there is no clock skew.)
   b. How much clock skew can the circuit tolerate before it experiences a hold time violation?

<table>
<thead>
<tr>
<th>Gate</th>
<th>Propagation delay (ps)</th>
<th>Contamination delay (ps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>AND</td>
<td>20</td>
<td>15</td>
</tr>
<tr>
<td>NOT</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>NOR</td>
<td>15</td>
<td>15</td>
</tr>
<tr>
<td>XNOR</td>
<td>30</td>
<td>20</td>
</tr>
</tbody>
</table>

D-FF CLK to Q Propagation delay: 35 ps
D-FF CLK to Q Contamination delay: 30 ps
D-FF Data setup time: 60 ps
D-FF Data hold time: 20 ps
3. Design a serial 2's complementer using a shift register, a single D-FF and minimum number of other gates. The binary number is shifted out from one side of the register and its 2's complement is shifted into the other side of the shift register.

2's complement of a number can be obtained by keeping the least significant bits the same until the first 1 is encountered and then complementing all the remaining bits. For example, two's complement of "00111100" is "11000100", where the underlined digits were unchanged by the copying operation (while the rest of the digits were flipped).

Start with designing an FSM, and then think about how to implement it using a shift register and a D-FF.
4. For the given circuit which has two 1 bit inputs (Y, Z) and two outputs (out_1, out_2):
   
a. Write the state table.
b. Draw the state diagram.
c. Describe the functionality of this FSM.
d. Is this a Mealy machine or a Moore machine?