1. Design a flip flop which has two control inputs called P and N. This PN flip flop performs the following operations:

   if \((P,N) = (0,0)\), reset the output to zero;
   if \((P,N) = (0,1)\), hold the previous output;
   if \((P,N) = (1,0)\), invert the previous output;
   if \((P,N) = (1,1)\), set the output to one.

   a. Fill out a truth table for this circuit
   b. Provide the characteristic equation for the PN flip flop
   c. Show how we can implement D-FF using this PN-FF
   d. Show how we can implement PN-FF using D-FF and other gates, muxes, etc.

2. For the circuit shown below, do the following:

   a. write a logic equation for the output and the next state
   b. write an excitation table (current state, inputs, next state, outputs)
   c. draw the state diagram
   d. draw the waveform for output P given the clock and D_in signal in figure below. Assume zero delay through all gates and D-FF, and reset signal not enabled. Assume initial state of D-FF to be zero.
   e. draw the waveform for output P for the same signals shown in part d., but now assuming it is a D-latch instead of D-FF. Assume zero delay through all gates and D-FF, and reset signal not enabled. Assume initial state of the latch to be zero.
3. Design a 4-bit register (to hold data) with capability of parallel load using only D-FFs, AND, OR gates and inverters. Register should hold the data in each cycle and load 4-bit input data in parallel when load signal is logic 1. Your design also should be able to set output P to logic 1 when the pattern “1101” is detected in the register.

4. Design a circuit consisting of 8-bit counters with selectable "up" and "down" modes. The circuit sets an output Y to 1 whenever the counter output has "10100" in its LSB bits i.e for counter output 00010100 and 11110100. Use 4-bit up-down counters as building blocks.