CSE 240A:
Principles of Computer Architecture
Professor: Michael Taylor

UCSD Department of Computer Science & Engineering

http://www.cse.ucsd.edu/classes/fa14/cse240A-a/
Computer Architecture from 10,000 feet

foo(int x)
{ .. }
Computer Architecture from 10,000 feet

foo(int x) { .. }

Class of application

An impossibly large gap!

In the olden days:

“In 1942, just after the United States entered World War II, hundreds of women were employed around the country as computers...” (source: IEEE)
The Great Battles in Computer Architecture Are About How to Refine the Abstraction Layers

foo(int x) { .. }

Computation
- Language
- Compiler
- ISA
- Micro Architecture
- Register-Transfer Level
- Circuits
- Devices
- Materials Science

Fortran
- IBM 360, VLIW
- RISC, T’meta
- Superscalar, caches

Mead & Conway

Physics
Abstractions protect us from change -- but must also change as the world changes.
Abstraction Layers - reflected in organization of research communities

**Computation**
- Language
- Compiler
- ISA
- Micro Architecture
- Reg-Transfer Level
- Circuits
- Devices
- Materials Science

**Physics**
- International Symposium on Computer Architecture (ISCA)
- High Performance Computer Architecture (HPCA)
- Architectural Support for Programming Languages and OS (ASPLOS)
- International Symposium on Microarchitecture (MICRO)
- Design Automation Conference (DAC)
- Int. Conf. Computer Aided Design (ICCAD)
- International Solid State Circuit Conference (ISSCC)
- International Electron Devices Meeting (IEDM)
Classic ISSCC (Circuits) Paper: "How we designed a chip and how fast / low power it is."

**TABLE IV**
Voltage/Frequency Schmoo

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**Freq (GHz)**

- 2
- 4
- 6
- 8
- 10
- 12
- 14
- 16
- 18
- 20
- 22
- 24
- 26
- 28
- 30
- 32
- 34
- 36
- 38
- 40
- 42
- 44
- 46
- 48
- 50
- 52

Failed
90 nm Generation Transistor

- Nickel Silicide Layer
- Silicon Gate Electrode
- 1.2 nm SiO₂ Gate Oxide
- Strained Silicon

No other company combines these transistor features at the 90 nm generation.

Intel

Figure 11: 1.2 nm gate oxide time to fail vs. electric field.

Figure 6: NMOS $I_{ON}$ vs. $I_{OFF}$ at 1.0V and 1.2V.
Classic Int. Electron Device Meeting (IEDM)
Paper: “How we designed a wire”
The focus of this class

Language
Compiler
ISA
Micro Architecture
Reg-Transfer Level
Circuits
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Materials Science

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International Electron Devices Meeting (IEDM)
Change: Power  
Santa Clara, we have a problem

More pipeline stages,  
less efficient, more power.

Just can’t remove  
> 100 watts  
without great expense on a desktop.

**All** computing is now  
**Low Power Computing!**
Power Density

Power doubles every 4 years
5-year projection: 200W total, 125 W/cm²!

P=VI: 75W @ 1.5V = 50 A!

From “New Microarchitecture Challenges in the Coming Generations of CMOS Process Technologies”
Change: microprocessor frequency versus time

Faster Circuits,
Faster + Smaller Transistors,
Fast Microarchitecture

Power Limited

Intel x86

7 yr / 10x (39%)
5 yr / 10x (58%)
20 yr / 10x (12%)
Intel

P3: 12 stages
P4 (b4 paper): 20 stages
P4/prescott: 31 stages
P5/Tejas: >> 31 stages
Intel

P3: 12 stages
P4 (b4 paper): 20 stages
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Intel

P3: 12 stages
P4 (b4 paper): 20 stages
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Back to the future

P3:
12 stages

P4 (b4 paper):
20 stages

P4/prescott:
31 stages

P5/Tejas:
31 stages

Same as 1996 – I can’t sell that. I must call it something new --- Pentium...Mmmm... Great Scott, I’ve got it!
And forward to multi-core

Intel Core Duo
Future outlook

Old Trend: Frequency

Current Trend: Parallel processing

Future Trend: Heterogeneity at all levels
- specialized coprocessors
- more and more materials
- stacking of dies from diff. fabs

→ Processors stuck at 4 GHz. Intel and others are pushing multi-core and specialization
Abstractions protect us from change -- but must also change as the world changes.

Changes in application space

- Language
- Compiler
- ISA
- Micro Architecture
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- Circuits
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Virtual Homicide (Quake)
Photographic memory
Telepathic
Mathematical Genius
Etc...

Physics
And on that note: PC’s are not the only important class of computer - in fact they are in the minority (~2%)!
Course Work and Grading

• See website!

http://www-cse.ucsd.edu/classes/fa14/cse240A-a/
Text vs. Lectures vs. Prereq (141)

Assigned readings for each lecture posted on website!

- Lectures will include material not in the text…text will include material not in the lectures. (Midterms and homework will give you an opportunity to calibrate what you need to know.)

- Resource limitations prevent us from addressing material from the prerequisite, CSE 141, in office hours…but we are happy to refer you to the book or your classmates.
Course Staff

Instructor: Michael Taylor
Email: mbtaylor@ucsd.edu
Office Hours:
EBU 3b 3202  
Tuesday right after class

TAs:

Moein
Shelby
About Me

PowerMush IV
PowerMush 3

x86 asm
Coding
68K
C

5 15 20 25 30
About Me

~120 million transistors
Course Outline

1. Technology
2. Measuring *Goodness*
3. Out-of-Order Superscalar
4. Memory Hierarchy
5. Power

Please watch the website for course updates, reading assignments and homework assignments!