Lecture 10:
Sequential Networks: Timing and Retiming

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Timing

• Two timing constraints: Shortest and longest timing paths
• Flip-Flop timing window
• Combinational timing
Timing

• Clock specifies a precise time for the next state
  – In general, we allocate one clock period for signal propagation between registers.
• Too late: Fail to reach for the setup of the next state.
• Too early: Race to disturb the holding of the next state.
• Analysis: Verify the timing of the system.
• Goal: A robust design.
So far ....

Combinational

CLK

Logic-level analysis
This lecture …

- When does our (seemingly logically correct) design go wrong?
- How can we design a circuit that works under real constraints?
A typical sequential network has combinational circuit between registers (R1 to R2).
The registers are synchronized by clocks (CLK1 to CLK2).
Timing is set between clocks (CLK1 and CLK2).
The beauty of the synchronized design is that we need only to take care of the timing of the regions separated by the registers.
For a synchronized digital Moore machine, we need to take care of the timing of the following region(s).
A. Between every pair of registers.
B. Between i. input and register, and ii. register and output.
C. Both A and B.
D. Whole system from input to output including registers.
$t_{cq} + t_{comb} + t_{setup} \leq T$

$t_{hold} < t_{cq} + t_{comb}$

$t_{cq}$: time from rising edge of clock to Q update ($CLK1 \Rightarrow B$)
$t_{comb}$: time of combinational logic delay ($B \Rightarrow C$)
$t_{setup}$: setup time before rising edge of clock ($C \Rightarrow CLK2$)
$t_{hold}$: hold time after the rising edge of clock
T: clock period ($CLK1 \Rightarrow CLK2$)
Setup time constraint

\[ t_{cq} + t_{comb} + t_{setup} \leq T \quad \Rightarrow \quad \text{max}(t_{cq} + t_{comb} + t_{setup}) \leq T \]

Hold time constraint

\[ t_{hold} < t_{cq} + t_{comb} \quad \Rightarrow \quad t_{hold} < \text{min}(t_{cq} + t_{comb}) \]

Longest delay from CLK1 to CLK2

Shortest delay from CLK1 to CLK2
Sequential Networks

Timing: Setup Time and Hold Time Constraints
Timing Constraints of flip flops

What if the input transition happens late, close to the rising edge?
A. Output will still be one at $t_1$
B. Output will be zero at $t_1$
C. Can’t say for sure
Input Constraints: Set up and hold time

I. Setup time: $t_{\text{setup}}$
   Time before the clock edge that data must be stable (i.e. not change)

II. Hold time: $t_{\text{hold}}$
   Time after the clock edge that data must be stable

Aperture time: $t_a$
Time around clock edge that data must be stable ($t_a = t_{\text{setup}} + t_{\text{hold}}$)
I. Setup time violation
   This occurs if the input data signal does not remain unchanged for at least $t_{\text{setup}}$ before the clock edge.

II. Hold time violation
   This occurs if the input data signal does not remain unchanged for at least $t_{\text{setup}}$ before the clock edge.
Output Timing Constraints

- Propagation delay: $t_{pcq} = \text{time after clock edge that the output } Q \text{ is guaranteed to be stable (i.e., to stop changing)}$

- Contamination delay: $t_{ccq} = \text{time after clock edge that } Q \text{ might be unstable (i.e., start changing)}$
Output Timing Constraints

I. Contamination delay: $t_{ccq}$
   Time after clock edge that $Q$ might be unstable (i.e., start changing)

II. Propagation delay: $t_{pcq}$
   Time after clock edge that the output $Q$ is guaranteed to be stable (i.e., to stop changing)
PIQ: A hold time violation is likely to occur when

A. The input signal (into the flip flop) fails to change to a desired value fast enough
B. The output signal (out of the flip flop) takes too long to stabilize
C. The input signal (into the flip flop) does not remain stable long enough after the clock edge
D. The output signal (out of the flip flop) changes too quickly
PIQ: The timing of which of the following signals can cause a setup-time violation?

A. The input signal T(t)
B. The output signal Q(t)
C. The clock signal, CLK
D. Some of the above
E. None of the above

Diagram:

- T(t) to T
- Q(t) to Q
- CLK to Q

Diagram with arrow labels:

- T(t) to T
- Q(t) to Q
- CLK to Q
PIQ: For a given flip-flop implementation which of its timing parameters can we modify when designing a sequential network (depicted below)

A. Set up and hold time
B. Propagation and Contamination delays
C. All of the above
D. None of the above
Fact 1: Once a flip flop has been ‘built’ we are stuck with its timing characteristics: $t_{\text{setup}}$, $t_{\text{hold}}$, $t_{\text{ccq}}$, $t_{\text{pcq}}$

Now let’s look at the timing characteristics of the combinational part.
Combinational Logic: Output timing constraints

I. Why don’t we have input constraints?
I. **Contamination delay**: $t_{cd}$

Minimum time from when an input changes until any output *starts* to change
Combinational Logic: Output timing constraints

I. Contamination delay: $t_{cd}$
   Minimum time from when an input changes until any output starts to change

II. Propagation delay: $t_{pd}$
   Maximum time from when an input changes until the output or outputs of a combinational circuit are guaranteed to reach their final value (i.e., stop changing)
PI Q: Which path in the above circuit determines the contamination delay of the circuit (assuming the delay of all the gates is the same)?

A. AND- OR – NOR
B. AND-OR
C. NOR
D. OR-NOR
PI Q: Which path in the above circuit determines the propagation delay of the circuit (assuming the delay of all the gates is the same)?

A. AND- OR – NOR
B. AND-OR
C. NOR
D. OR- NOR
An alternate view of the sequential circuit
What should happen within a clock cycle for correct functionality?
The delay between registers has a **minimum** and **maximum** delay, dependent on the delays of the circuit elements (Dynamic Discipline)
PI Q: Suppose input to R1 changed before \( t_1 \), what is the maximum delay (from \( t_1 \)) after which D2 reaches a stable value?

A. Setup time of R1+ Propagation delay of CL + Propagation delay of R2
B. Hold time of R1+ Propagation delay of CL + setup time of R1
C. Propagation delay of R1+ Propagation delay of CL + Propagation delay of R2
D. Propagation delay of R1+ Propagation delay of CL
E. Propagation delay of CL + Propagation delay of R2
Setup Time Constraint

- The setup time constraint depends on the **maximum** delay from register R1 through the combinational logic.
- The input to register R2 must be stable at least $t_{\text{setup}}$ before the clock edge.

Maximal delay, $t_{\text{max}}$

\[
\text{Setup Time Constraint:}
\]
Setup Time Constraint

\[ T_c \geq t_{pcq} + t_{pd} + t_{\text{setup}} \]

PI Q: As a designer, which of the following parameters would you modify to meet the set up time constraint?

A. The clock period, \( T_c \)
B. The prop. delay of R1, \( t_{pcq} \)
C. The prop. delay of CL, \( t_{pd} \)
D. The setup time of R2, \( t_{\text{setup}} \)
E. All of the above
Setup Time Constraint

\[ T_c \geq t_{pcq} + t_{pd} + t_{\text{setup}} \]

\[ t_{pd} \leq T_c - (t_{pcq} + t_{\text{setup}}) \]

PI Q: As a designer, which of the following parameters would you modify to meet the set up time constraint?

A. The clock period, \( T_c \)
B. The prop. delay of R1, \( t_{pcq} \)
C. The prop. delay of CL, \( t_{pd} \)
D. The setup time of R2, \( t_{\text{setup}} \)
E. All of the above
PI Q: Suppose input to R1 changed before $t_1$, what is the minimum delay (from $t_1$) after which D2 starts to change?

A. Setup time of R1 +
   propagation delay of CL +
   propagation of R2
B. Hold time of R1 +
   propagation time of CL
   + setup time of R1
C. Hold time of R1 +
   Contamination delay of CL +
   Propagation time of R2
D. Contamination delay of R1 +
   Contamination delay of CL
E. Contamination delay of CL +
   Contamination delay of R2
Hold Time Constraint

- The hold time constraint depends on the *minimum* delay from register R1 through the combinational logic.
- The input to register R2 must be stable for at least $t_{\text{hold}}$ after the clock edge.

Minimum delay, $t_{\text{min}}$

Hold Time Constraint:
Hold Time Constraint

\[ t_{\text{hold}} < t_{ccq} + t_{cd} \]

\[ t_{cd} > t_{\text{hold}} - t_{ccq} \]
Timing Analysis

Timing Characteristics

\[ t_{ccq} = 30 \text{ ps} \]
\[ t_{pcq} = 50 \text{ ps} \]
\[ t_{setup} = 60 \text{ ps} \]
\[ t_{hold} = 70 \text{ ps} \]
\[ t_{pd} = 35 \text{ ps} \]
\[ t_{cd} = 25 \text{ ps} \]

Setup time constraint:
\[ T_c \geq f_c = 1/T_c \]

Hold time constraint:
\[ t_{ccq} + t_{pd} > t_{hold} ? \]
Timing Analysis

Timing Characteristics

- \( t_{ccq} = 30 \text{ ps} \)
- \( t_{pcq} = 50 \text{ ps} \)
- \( t_{setup} = 60 \text{ ps} \)
- \( t_{hold} = 70 \text{ ps} \)
- \( t_{pd} = 35 \text{ ps} \)
- \( t_{cd} = 25 \text{ ps} \)

Setup time constraint:

\[ T_c \geq (50 + 105 + 60) \text{ ps} = 215 \text{ ps} \]

\[ f_c = \frac{1}{T_c} = 4.65 \text{ GHz} \]

Hold time constraint:

\[ t_{ccq} + t_{cd} > t_{hold} ? \]

\[ (30 + 25) \text{ ps} > 70 \text{ ps} ? \] \text{No!}
Fixing Hold Time Violation

Add buffers to the short paths:

CLK

A

B

C

D

CLK

X

Y

X'

Y'

Setup time constraint:

\[ T_c \geq f_c \]

Hold time constraint:

\[ t_{ccq} + t_{pd} > t_{hold} \]

Timing Characteristics

\[ t_{ccq} = 30 \text{ ps} \]
\[ t_{pcq} = 50 \text{ ps} \]
\[ t_{setup} = 60 \text{ ps} \]
\[ t_{hold} = 70 \text{ ps} \]
\[ t_{pd} = 35 \text{ ps} \]
\[ t_{cd} = 25 \text{ ps} \]
Fixing Hold Time Violation

Add buffers to the short paths:

\[ t_{pd} = 3 \times 35 \text{ ps} = 105 \text{ ps} \]
\[ t_{cd} = 2 \times 25 \text{ ps} = 50 \text{ ps} \]

Setup time constraint:
\[ T_c \geq (50 + 105 + 60) \text{ ps} = 215 \text{ ps} \]
\[ f_c = 1/T_c = 4.65 \text{ GHz} \]

Hold time constraint:
\[ t_{ccq} + t_{cd} > t_{hold} ? \]
\[ (30 + 50) \text{ ps} > 70 \text{ ps} ? \text{ Yes!} \]
Clock Skew

- The clock doesn’t arrive at all registers at the same time
- Skew is the difference between two clock edges
- Examine the worst case to guarantee that the dynamic discipline is not violated for any register – many registers in a system!
Setup Time Constraint with Clock Skew

- In the worst case, the CLK2 is earlier than CLK1

\[ T_c \geq t_{pcq} + t_{pd} + t_{setup} + t_{skew} \]

\[ t_{pd} \leq T_c - (t_{pcq} + t_{setup} + t_{skew}) \]
Timing Analysis with clock skew

Timing Characteristics

\[ t_{ccq} = 30 \text{ ps} \]
\[ t_{pcq} = 50 \text{ ps} \]
\[ t_{\text{setup}} = 60 \text{ ps} \]
\[ t_{\text{hold}} = 70 \text{ ps} \]
\[ t_{pd} = 35 \text{ ps} \]
\[ t_{cd} = 25 \text{ ps} \]
\[ t_{\text{skew}} = 50 \text{ ps} \]

\[ T_c \geq 265 \text{ ps} \]
\[ f_c = \frac{1}{T_c} = 3.77 \text{ GHz} \]

Without skew we got \[ f_c = 4.65 \text{ GHz} \]
Hold Time Constraint with Clock Skew

• In the worst case, CLK2 is later than CLK1

\[ t_{ccq} + t_{cd} > t_{\text{hold}} + t_{\text{skew}} \]
\[ t_{cd} > t_{\text{hold}} + t_{\text{skew}} - t_{ccq} \]
Hold Time Violation

Add buffers to the short paths:

Timing Characteristics

- $t_{ccq} = 30 \text{ ps}$
- $t_{pcq} = 50 \text{ ps}$
- $t_{setup} = 60 \text{ ps}$
- $t_{hold} = 70 \text{ ps}$
- $t_{pd} = 35 \text{ ps}$
- $t_{cd} = 25 \text{ ps}$
- $t_{skew} = 50 \text{ ps}$

$tpd = 3 \times 35 \text{ ps} = 105 \text{ ps}$

$t_{cd} = 2 \times 25 \text{ ps} = 50 \text{ ps}$

Hold time constraint:

$t_{ccq} + t_{cd} > t_{hold} + t_{skew}$?

$(30 + 50) \text{ ps} > (70 \text{ ps} + 50) \text{ ps}$?
Timing and Retiming

- Retiming: Adjust the clock skew so that the clock period can be reduced.
- Add a few more examples on timing and retiming.
Conclusion

• Clock to Clock: Range of shortest and longest paths
• Design revision and retiming to adjust the constraints
• Research: Variation aware designs