Lecture 1:
Introduction to Digital Logic Design

CSE 140: Components and Design Techniques for Digital Systems
Fall 2014

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Information about the Instructor

- Instructor: CK Cheng
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- Industrial Exp: Consultant, Engineer of AMD, Mentor Graphics, Bellcore
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- Office hours will be posted on the course website
Information about TAs

• Ilgweon Kang, <i1kang@eng.ucsd.edu>
• Howard Hao Zhuang <hao.zhuang@cs.ucsd.edu>
• Dao D Lam <d2lam@ucsd.edu>

Office hours will be posted on the course website
Logistics: Resources

All information about the class is on the class website:
http://cseweb.ucsd.edu/classes/fa14/cse140-b/index.html

• *Approx. Syllabus*
• Detailed schedule
• Readings
• Assignments (TED)
• Grading policy (Website)
• Forum (Piazza)
• Content/announcements and grades will be posted through Piazza *make sure you have access

I will assume that you check these daily
Logistics: Textbooks

Required text:


Other references:

- [Lang]: “Digital Systems and Hardware/Firmware Algorithms” by Milos D. Ercegovac and Tomas Lang
Lecture: Peer Instruction

• I will pose carefully designed questions. You will
  – Solo vote: Think for yourself and select answer
  – Discuss: Analyze problem in teams of three
    • Practice analyzing, talking about challenging concepts
    • Reach consensus
    • If you have questions, raise your hand and I will come over
  – Group vote: Everyone in group votes
  – Class wide discussion:
    • Led by YOU (students) – tell us what you talked about in
discussion that everyone should know!
Logistics: Course Components

Grading (grade on style, completeness and correctness)

• iClicker: x% (10 out of 15 classes), $x=5$ voted by class
• Homework: 9-x% (grade based on a subset of problems. If more than 70% of class fills CAPEs, best 4 out of 5 )
• Midterm 1: 30% (T 10/28)
• Midterm 2: 30% (T 11/18)
• Midterm 3: 30% (Th 12/11)
• Take home final exam: 1% (due 230PM, F 12/19)
• Grading: The best of
  – Absolute: A- >90% ; B- >80% of total score (100%).
  – The curve: (A+,A-) top $33+\varepsilon\%$ of class; (B+,B-) second $33+\varepsilon\%$
  – The bottom: C- > 45% of total score.
A word on HWs and exams

• HWs:
  – Practice for exams
  – Do them individually for best results

• Exams
  • (Another) Indication of how well you have absorbed the material
  • Solution and grading policy will be posted after exam.
  • Learn from mistakes and move on ….
Course Problems...Cheating

• What is cheating?
  – Studying together in groups is **encouraged**
  – Turned-in work must be *completely* your own.
  – Copying someone else’s solution on a HW or exam is cheating
  – Both “giver” and “receiver” are equally culpable

• We have to address the issue once the cheating is reported by TAs or tutors.
Motivation

• Microelectronic technologies have revolutionized our world: cell phones, internet, rapid advances in medicine, etc.

• The semiconductor industry has grown from $21 billion in 1985 to $315 billion in 2013.
The Digital Revolution

Integrated Circuit: Many digital operations on the same material

Vacuum tubes

ENIAC

Stored Program Model

WWII

Integrated Circuit

1949

1965

Moore’s Law

Exponential Growth of Computation

(1.6 x 11.1 mm)
Robert Noyce, 1927 - 1990

- Nicknamed “Mayor of Silicon Valley”
- Cofounded Fairchild Semiconductor in 1957
- Cofounded Intel in 1968
- Co-invented the integrated circuit
Gordon Moore

• Cofounded Intel in 1968 with Robert Noyce.
• Moore’s Law: the number of transistors on a computer chip doubles every 1.5 years (observed in 1965)
Since 1975, transistor counts have doubled every two years.
Principle of Abstraction

Abstraction: Hiding details when they aren’t important
Scope

• The purpose of this course is that we:
  – Learn the principles of digital design
  – Learn to systematically debug increasingly complex designs
  – Design and build digital systems
  – Learn what’s under the hood of an electronic component
We will cover four major things in this course:

- Combinational Logic (Harris-Chap 2)
- Sequential Networks (Harris-Chap 3)
- Standard Modules (Harris-Chap 5)
- System Design (Harris-Chap 4, 6-8)
Scope: Overall Picture of CS140

Data Path Subsystem
- Memory File
- ALU
- Memory Register
- Conditions

Control Subsystem
- Conditions
- Sequential machine
- Control
- CLK: Synchronizing Clock
Combinational Logic vs Sequential Network

**Combinational logic:**

\[ y_i = f_i(x_1, \ldots, x_n) \]

**Sequential Networks**

1. **Memory**
2. **Time Steps (Clock)**

\[ y_i^{t+1} = f_i(x_1^t, \ldots, x_n^t, s_1^t, \ldots, s_m^t) \]

\[ S_i^{t+1} = g_i(x_1^t, \ldots, x_n^t, s_1^t, \ldots, s_m^t) \]
## Scope

<table>
<thead>
<tr>
<th>Subjects</th>
<th>Building Blocks</th>
<th>Theory</th>
</tr>
</thead>
<tbody>
<tr>
<td>Combinational Logic</td>
<td>AND, OR, NOT, XOR</td>
<td>Boolean Algebra</td>
</tr>
<tr>
<td>Sequential Network</td>
<td>AND, OR, NOT, FF</td>
<td>Finite State Machine</td>
</tr>
<tr>
<td>Standard Modules</td>
<td>Operators, Interconnects, Memory</td>
<td>Arithmetics, Universal Logic</td>
</tr>
<tr>
<td>System Design</td>
<td>Data Paths, Control Paths</td>
<td>Methodologies</td>
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Part I. Combinational Logic

Next Lecture Reading:
[Harris] Chapter 2, Section 2.1-2.4