CSE140 - HW #5

Due Wednesday December 10, 5:00PM

(I). System Design: Implement the following algorithm:

Alg(X,Y,Z,req,ack)
Input X[7:0], Y[7:0], req;
Output Z[7:0], ack;
Local-object A[7:0], B[7:0];
S1: if req’ goto S1 || ack <= 1;
S2: ack <= 0 || A <= X || B <= Y;
S3: if (A > 0) goto S5;
S4: A <= A+B || goto S3;
S5: Z <= A || ack <= 1 || goto S1;
end Alg

(1). Design a data subsystem that is adequate to execute the algorithm and draw the schematic diagram.
(2). Design the control subsystem (i) draw the state diagram; (ii) implement the control subsystem with the style of one hot encoding. Draw the logic diagram to demonstrate the design.

(II). System Design: Implement the following algorithm:

Alg(X,Y,req,W,U,ack)
Input X[7:0], Y[7:0], req;
Output W[7:0], U[7:0], ack;
Local-object A[7:0], B[7:0], C[3:0], D[7:0];
S1: If req’ goto S1 || ack <= 1;
S2: ack <= 0 || A <= X || B <= Y || C <= (0111) || D <= Clear(D);
S3: if (A < B) goto S5;
S4: A <= A-B || D <= D+1
S5: if (C==0) goto S7 || C <= C-1;
S6: B <= Shift(B,R,1) || D <= Shift(D,L,1) || goto S3;
S7: W <= A || U <= D || ack <= 1 || goto S1;
End Alg

(1). Design a data subsystem that is adequate to execute the algorithm. Draw the schematic diagram to show the design.
(2). Design the control subsystem (i) draw the state diagram; (ii) implement the control subsystem with the style of one hot encoding. Draw the logic diagram to demonstrate the design.