Please read the following instructions carefully: The exam contains 6 problems of which we are free to choose four or more to answer. The grade will be counted according to the best four. This is an open book final. Web searches are encouraged. If there is any uncertainty about the problems, make and state your assumptions. The final should be done individually. Therefore, no discussion or collaboration is allowed.

1. Boolean algebra and switching algebra: The problem is about the scope of Boolean algebra and switching algebra and their difference.

1.1 State the difference between Boolean algebra and switching algebra. Use an example to demonstrate the difference.

1.2 Suppose that \( A + B = A \) and \( AB = B \) in Boolean algebra, what can be claimed about \( B \) as a function of \( A \)?

1.3 Suppose that \( A + B = A \) and \( AB = 0 \) in switching algebra, what can be claimed about \( B \) as a function of \( A \)?

2. Two Level Logic Minimization: The problem is about the theory and implementation of logic minimization. Given a switching function with on-set \( F = \{ f_i \} \), don't-care set \( D = \{ d_i \} \) and off-set \( R = \{ r_i \} \), where each \( f_i, d_i, \) or \( r_i \) is a product term. We want to generate all possible prime implicants for two level logic minimization.

2.1. State the definition of the prime implicant.

2.2. Suppose that you are the chief software engineer. We need a high level pseudo code to generate all prime implicants \( p_i \). Write the pseudo code and explain your algorithm. Hint: Assume that you have some low level routines available for the pseudo code. Some (not all) possible routines are listed below. You may define and use similar routines in your algorithm.

- \( \text{adjacency}(p_i, p_j) \): returns true if product terms \( p_i \) and \( p_j \) are adjacent, otherwise returns false.
- \( \text{consensus}(p_i, p_j) \): returns the consensus if the two product terms \( p_i \) and \( p_j \) are adjacent, otherwise returns an empty set.
- \( \text{tautology}(S) \): The set \( S \) contains a list of product terms. This routine returns true if the sum of all product terms in the set \( S \) is always true for any input combination, otherwise the routine returns false.

3. Shannon’s Expansion: This problem is about the proof and application of Shannon’s expansion to Boolean satisfiability problem.

3.1. Prove the Shannon’s expansion theorem of switching algebra.

3.2. Boolean Satisfiability Problem: Given a nine variable switching function,

\[
F(a, b, c, d, e, f, g, h, i) = abc + abd + acd + ace + ade + adf + a'ef + a'eg + a'fg + a'fh + a'gh + a'gi + bc'd + bce + bd'e + bd'f + be'g + b'eg + b'f'g + b'fh + b'g'h + b'g'i + e'f'g' + e'fh' + e'gi' + e'gh' + f'g'i' + fh' + g'hi' + fh'i' .
\]

Find one binary assignment of the input variables so that function \( F = 0 \). Explain your derivation if you can or cannot find a solution.
4. Timing: The problem is about the timing and retiming of digital logic. The logic diagram of Figure 5.18c in the book of Harris and Harris shows a $4 \times 4$ multiplier. Suppose the inputs $A, B$ and output $P$ are locked by registers.

4.1. Suppose that the inputs $A = (1011)$ and $B = (1101)$, write the content of the output $P[7 : 0]$.

4.2. The timing characteristics of the components are summarized below.

- Flip-flop: clock-to-Q maximum delay $t_{pcq} = 35\text{ps}$, clock-to-Q minimum delay $t_{ccq} = 20\text{ps}$, setup time $t_{setup} = 30\text{ps}$, hold time $t_{hold} = 20\text{ps}$
- Logic gate: AND: propagation delay $t_{pd} = 35\text{ps}$, contamination delay $t_{cd} = 15\text{ps}$.
- Logic gate: Full Adder:
  - $C_{in}$ to either output: propagation delay $t_{pd} = 20\text{ps}$, contamination delay $t_{cd} = 15\text{ps}$.
  - $A$ or $B$ to $Sum$: propagation delay $t_{pd} = 30\text{ps}$, contamination delay $t_{cd} = 22\text{ps}$.
  - $A$ or $B$ to $C_{out}$: propagation delay $t_{pd} = 25\text{ps}$, contamination delay $t_{cd} = 22\text{ps}$.

4.2.1. Derive the minimum clock period without clock skew.

4.2.2. Suppose that the input and output are driven by different clocks. Derive the skew between the clocks to minimize the clock period.

5. Sequential machines: The problem is about the specification and design of a sequential machine. You have been enlisted to improve the traffic controller at the intersection of Academic Avenue and Bravado Blvd. as shown in Figure 3.23 of the book by Harris and Harris. Due to heavier traffic, we need to add left turn signals on both streets.

5.1. Show your state diagram.

5.2. Design the logic diagram with a minimal number of flip-flops.

5.3. Design the logic diagram using one-hot machine designs.

5.4. Compare the above two designs in terms of the number of flip-flops and number of logic gates.

6. System Design: The problem is about the system design from a given specification. Follow the IEEE 754 single format with a 32-bit word size. Let us assume that the two numbers are positive and ignore the subnormal cases and round off errors. Design a floating point addition using a datapath and control subsystem methodology.

6.1 Describe your algorithm.

6.2 Describe the data subsystem with a schematic diagram.

6.3 Draw the state diagram of the control subsystem and list the control signals generated by the control subsystem.