2013 Fall CSE140L

*Digital Systems Laboratory*

Lecture #3

by

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Welcome to Verilog
module module_name ( port specification... );

local wires, variables declaration;
task, function declaration;  

continuous assignments ;  // for mainly combinational circuit
procedural blocks;  // for mainly sequential circuit
instantiation of modules;  // for hierarchical design
instantiation of primitives /UDP;  // for built-in primitives

endmodule
Introduction to Verilog HDL (Home work)

Warning about incorrect information on documents:

Electronics, CAD Technology and Verilog HDL keep changing continuously. Therefore some information contained in the following documents (or any document in general) may be incorrect and not working. For our FA13 CSE140L class, only way to verify the correctness of the information is to test any information by simulating, compiling and testing using our CAD SW (Altera Quartus II Web Edition Software v9.0 Service Pack 2) on DE1 board.

1. **[Quartus II example practice using Verilog]**: (Note: You can do this example without understanding of Verilog.) Follow the instructions described in [tut_quartus_intro_verilog_de1](#).

2. **[Verilog Tutorial for beginner]**: Follow [Verilog short tutorial](#) to make yourself familiar with this new design entry methodology.

3. **[Manual]**: [intro_verilog_manual](#)

4. **[Quick Reference Card]**: [Two-page Card](#), [Multiple-page Card](#)

5. In addition, there are numerous Verilog information & tutorials available on the web in doc, book, & video format. The [Verilog on wiki](#) is an excellent place to learn the language. It also lists many tutorial links that student may visit and learn.