Microprocessor Packaging

The Key Link in the Chain

Koushik Banerjee
Technical Advisor
Assembly Technology Development
Intel Corporation
Microprocessors

1971

2001
Main R&D facility in Chandler, AZ
Computing needs driving complexity

First to introduce organic in mainstream CPUs

First to introduce flip chip in mainstream CPUs

25 MHz 1.0+ GHz

Ceramic To Organic

Wire-bond To Flip Chip
Looking ahead ...

Complexity and Challenges to support Moore’s Law

1. Silicon to package interconnect
2. Within package interconnect
3. Power management
4. Adding more functionality

Goal: Bring technology innovation into High volume manufacturing at a LOW COST
Silicon & Package Relationship

Anatomy 101

Silicon Processor:
The "brain" of the computer (generates instructions)

Packaging:
The rest of the body (Communicates instructions to the outside world, adds protection)

No Package = No Product! Great Packaging = Great Products!!
The Key Link in the Chain

Opportunity
Innovative, efficient, high performance, low-cost packages are a significant competitive advantage
Example – Enabling Custom solutions

Value Add: custom solutions based on market segment
Breaking Barriers to Moore’s Law

The Number of Transistors Per Chip will Double Every 18 Months

Integrated Packaging + Silicon Technology development is essential

Source: Intel
Challenge # 1

Silicon to package interconnect
Approaching 10K flip chip bumps on a die

Driver – increased silicon functionality

Driver – increased silicon functionality

Flip Chip (C4) interconnect

Underfill

Silicon

Package

Number of flip chip bumps

10K

0

Pentium III® Family

Pentium 4® Family

Itanium™ Family

Future generations

Future generations

Driver – increased silicon functionality
Solution: Aggressive Bump Pitch Scaling to keep down die size

Key Challenges:
- Plating bumps
- Chip Attach Process
- Underfill
- Joint integrity
- HVM scalable process
Which leads us to ...

Challenge # 2

Within package Interconnect
Solution: High Density Interconnect

Driver: Need high wiring density

Very high escape routing density from the die

Lines narrower than hair

Human Hair

Package Traces
Dimensional Stack-Up

Line in Silicon
130 nm
(100X magnification)

Line in Package
25 um
(100X magnification)

Line in Motherboard
5 mils (0.005”)
(100X magnification)
Approaching 40K micro vias inside a package

Driver – High I/O count & power supply
Solution: Advanced lithography (new term in packaging!)

Key Challenges:
- Developing HDI (high density interconnect) at LOW COST
- High Volume Manufacturing Capable
Core frequency trend ... doubling every 2 years

In addition ...

Source : Intel Architecture Labs
FSB frequency ramp continues

Max Mega transfers / second

- Pentium® II Processor: 66
- Pentium® III Processor: 133
- Pentium® 4 Processor: 400
- Future Generation Processors

Microprocessor Generation
Solution: High Performance Interconnect Technology

Benefits of organic

1. Copper – Low resistance
2. Low dielectric constant
3. Cheaper

Key Challenge:

- Optimize the entire substrate architecture (material properties, layer stack-up, via placement, power bussing etc.)
Key Challenges:
- Signal Timing
- Innovative routing – layout
- Optimizing power / ground distribution
- Co-design of the complete silicon & package interconnect

A poor design can ruin processor performance.
Switching gears from interconnect to ...

Challenge # 3

Power Management
Power Increasing, silicon getting smaller

Two Challenges …
Getting power in & getting heat out

Source: Intel Architecture Labs
Importance of a quiet Power Supply

Ideal state

Reality – noise

This is what Voltage Scaling can do

High
Low

High
Low

High
Low

OR
OR
Need lots of charge, very quickly …

Increasing distance from supply

Hot Water Heater

Inefficient design

Still Waiting !!

Close Proximity to supply
Solution: Optimize design for power delivery

Key Challenge:

- 2X improvement in capacitance and inductance needed / generation
- Need to optimize the complete silicon package integrated power delivery solution
Solution: Reduce system design burden – heat removal

Temp – Silicon (T_J)  Temp – Package Case (T_C)  Temp – Ambient (T_A)

Packaging Provide Solutions for this interface of the budget

Temperature Gradient

OEM Provide Solutions for this interface of the budget

Integrated Thermal Solutions in the package reduce heat flux – easier to cool in the system
Example: Pentium4®

Integrated High Conductivity Heat Spreader

High conductivity Thermal Interface Material
Example: Itanium®

Integrated heat pipe technology interfacing directly to the silicon

Schematic of how a typical heat pipe works:
- Wick Structure
- Water Vapor
- Heater Block
- Vapor Condenses
- Cooler Section Of Heat Pipe
- Condensed water flows back through the wick structure by capillary action
And finally ...

Challenge # 4

Adding more functionality
Solution: High Density Interconnect = more integration

High Density Interconnect enables a large cache memory integration in a small space

Leveraging packaging instead of adding onto silicon
Solution: Massive integration = more features

On CPU Voltage regulation

RASM
In Summary ...
We talked about future Complexity and Challenges to support Moore’s Law

1. Silicon to package interconnect
2. Within package interconnect
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Intel’s Packaging Strategy

**Innovative Technology**
Making Technology **Affordable**
Smart designs
Integrated silicon + packaging solutions
For more information, please visit ….

http://www.intel.com/research/silicon/packaging.htm

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