From: Louis Lau <cape@ucsd.edu>
Date: Thu, Nov 8, 2012 at 10:22 PM
Subject: CAPE Instructions FA12
To: marthaucsd@gmail.com

To Fall 2012 Instructors,

The Course and Professor Evaluations (CAPE) this quarter will be available to students from:

**Monday, November 26 to Monday, December 10** (approx. Week 9 through Week 10).

**Student must complete their evaluations BEFORE Monday 8AM of Finals Week.**
**No exceptions.**

**HOW IT WORKS:** On the Monday of 9th week, each student will be given access by email to their evaluation webpage. Students will be prompted to separately evaluate each of their listed instructors for each enrolled course. Several reminder emails will be sent to students with uncompleted evaluations. CAPE will provide updated student response rate percentages throughout the evaluation period on our website at [cape.ucsd.edu](http://cape.ucsd.edu).

**RESULTS:** Statistics and numerical ratings will be posted online onto the CAPE website and the Schedule of Classes. Written student comments will be emailed to the corresponding academic department CAPE liaisons [http://www.cape.ucsd.edu/liasons/cape-liason-list.html](http://www.cape.ucsd.edu/liasons/cape-liason-list.html) after grades are posted.

**WHAT YOU NEED TO DO:** Historically, instructors who actively and creatively promote student participation in CAPE (especially throughout Weeks 9 and 10) receive more informative feedback on their teaching and curriculum. Please visit "Tips On Increasing Response Rate" at [www.cape.ucsd.edu/faculty/tips.html](http://www.cape.ucsd.edu/faculty/tips.html) to see what some faculty with high response rates have done.
LAB, STUDIO, SEMINAR FORMS: Your course is a lab, studio, or seminar? We have a form for that! With faculty and department assistance, we developed forms to replace the CAPE standard form for labs, studio classes, and seminar classes. Please email us by Friday, November 16th if you are interested in using one of these forms instead of the standard form. These forms and the standard form can be found on our website.

CUSTOM QUESTIONS: If you would like to pose specific questions to your students, please email up to 5 rating-type questions to cape@ucsd.edu with the course number and the instructor's name. These questions must be posed with a "strongly agree to strongly disagree" scale in mind. The deadline to provide us with the properly formatted questions is Friday, November 16th.

More information can be found at http://www.cape.ucsd.edu. If you have any questions or suggestions, please contact us.

Thank you for your support,
Aaron Louie and
Martha Carbajal
CAPE Director
LAB#3: Vending Machine Controller Design

• It has many states – Init, zero cents, 5 cents, 10 cents, ....
• How to move from one state to other state?
• How to detect & handle dispensing?
• How to detect & handle One-dollar bill, credit-card and coin input?
• How to handle Return and “Use Exact Change Only” operations?
• ....
Mealy vs. Moore FSM

Mealy Machine: \( y(t) = f(x(t), s(t)) \)
Moore Machine: \( y(t) = f(s(t)) \)

\( s(t+1) = g(x(t), s(t)) \)

Mealy Machine

\[
\begin{align*}
C1 \quad & \quad \text{CLK} \quad & \quad C2 \\
\downarrow \quad & \quad \uparrow \quad & \quad \downarrow \\
\text{x(t)} \quad & \quad \text{y(t)} \\
\end{align*}
\]

Moore Machine

\[
\begin{align*}
C1 \quad & \quad \text{CLK} \quad & \quad C2 \\
\downarrow \quad & \quad \uparrow \quad & \quad \downarrow \\
\text{x(t)} \quad & \quad \text{y(t)} \\
\end{align*}
\]
FSM design example – Moore vs. Mealy

A circuit which removes one $1$ (i.e., the first 1) from every string of 1s on the input stream:

<table>
<thead>
<tr>
<th>input</th>
<th>output</th>
</tr>
</thead>
<tbody>
<tr>
<td>..... 00000...... =&gt; ..... 00000......</td>
<td></td>
</tr>
<tr>
<td>..... 01010...... =&gt; ..... 00000......</td>
<td></td>
</tr>
<tr>
<td>..... 00110...... =&gt; ..... 00100......</td>
<td></td>
</tr>
<tr>
<td>..... 01110...... =&gt; ..... 01100......</td>
<td></td>
</tr>
<tr>
<td>..... 11011...... =&gt; ..... 10010......</td>
<td></td>
</tr>
</tbody>
</table>
FSM design example – Moore vs. Mealy

- Remove one 1 from every string of 1s on the input.
Moore FSM Verilog model: (Not necessary working solution)

```verilog
module reduce (input clk, in,
                output reg out);

parameter zero = 2'b00, one1 = 2'b01, two1s = 2'b10;
reg[2:1] state, next_state;

always @(posedge clk) begin
    state = next_state;
end

always @(in, state) begin
    case (state)
        zero: begin
            out = 0;
            if (in) next_state= one1;
            else next_state= zero;
        end
        one1: begin
            out = 0;
            if (in) next_state= two1s;
            else next_state= zero;
        end
        two1s: begin
            out = 1;
            if (in) next_state= two1s;
            else next_state= zero;
        end
    endcase
endmodule
```

Lecture #7
Mealy FSM Verilog model: (Not necessary working solution)

module reduce (input clk, in,
                        output reg out);

parameter zero = 1'b0, one = 1'b1;
reg state, next_state;

always @(posedge clk) begin
    state = next_state;
end

always @(in, state) begin
    case (state)
        zero: begin
            out = 0;
            if (in) next_state= one;
            else next_state= zero;
        end
        one: begin
            out = 0;
            if (in) begin
                out = 1;
                next_state= one;
            end
            else begin
                out = 0;
                next_state= zero;
            end
        end
    endcase
end

end module