2012 Fall  CSE140L

Digital Systems Laboratory

Lecture #3

by

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Simulation Input Waveforms

What waveform(s) should be used for inputs for simulation? For example in LAB#1 where we have three inputs SW0, SW1 and SW2.
LAB#1 Structure

You can organize it something like this so its easier to read/reason

- Thinh
ALU

Arithmetic Logic Unit (ALU) is a digital circuit that performs arithmetic and logical operations.

Question: Can we design it with combinational circuit?
Welcome to Verilog
Verilog in one slide!
By Choon Kim

```verilog
module module_name ( port specification... );

local wires, variables declaration;
task, function declaration;

continuous assignments ;  // for combinational circuit
procedural blocks;  // for sequential circuit
instantiation of modules ;  // for hierarchical design
instantiation of primitives /UDP;  // for built-in primitives

endmodule
```
Introduction to Verilog HDL

Home work (Reading materials)

Warning:
Some information contained in the following reading materials (or any material in general) may be incorrect and not working. Only way to verify the correctness of the information is to test it by simulating and synthesizing using our Altera Quartus SW & HW kit.

1. [Quartus II example with Verilog]: Note: You can do this without understanding of Verilog. Follow the instructions described in tut_quartus_intro_verilog_de1. This is the same homework in Lecture#1 except Verilog is used as a design entry instead of Schematic diagram.

2. [Tutorial for beginner]: Follow Verilog short tutorial to make yourself familiar with this new design entry methodology.

3. [Manual]: intro_verilog_manual

4. [Short Reference Card]: Two-page Card Multiple-page Card

5. In addition, there are numerous Verilog information & tutorials available on the web in doc, book, & video format. The Verilog on wiki is an excellent place to learn the background. This Verilog Tutorial is one of tutorial sites. You can use whatever you feel comfortable.