CSE 140 Lecture 12
Standard Combinational Modules

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Part III - Standard Combinational Modules (Chapter 5)

**Signal Transport**
- Decoder: Decode address
- Encoder: Encode address
- Multiplexer (Mux): Select data by address
- Demultiplexer (DeMux): Direct data by address
- Shifter: Shift bit location

**Data Operator**
- Adder: Add two binary numbers
- Multiplier: Multiply two binary numbers
Interconnect: Decoder, Encoder, Mux, DeMux

Processors

Arbiter

Memory Bank

Data

Address

Data

Address

Data

Address

Data

Address

Data

Address

Data

Address

Data

Address

Data

Address

Data
1. Decoder

- Definition
- Logic Diagram
- Application (Universal Set)
- Tree of Decoders
**iClicker: Decoder Definition**

A. A device that decodes
B. An electronic device that converts signals from one form to another
C. A machine that converts a coded text into ordinary language
D. A device or program that translates encoded data into its original format
E. All of the above
Decoder Definition: A digital module that converts a binary address to the assertion of the addressed device

EN (enable)

I₀ → 0
I₁ → 1
I₂ → 2

yᵢ = 1 if En = 1 & (I₂, I₁, I₀) = i
yᵢ = 0 otherwise

n inputs
n = 3

2ⁿ outputs
2³ = 8

n to 2ⁿ decoder function:
1. Decoder: Definition

- $N$ inputs, $2^N$ outputs
- One-hot outputs: only one output HIGH at once

<table>
<thead>
<tr>
<th>$A_1$</th>
<th>$A_0$</th>
<th>$Y_3$</th>
<th>$Y_2$</th>
<th>$Y_1$</th>
<th>$Y_0$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
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Decoder: Logic Diagram

\[ y_i = m_i \, En \]

\[ y_0 = 1 \text{ if } (I_2, I_1, I_0) = (0,0,0) \text{ and } En = 1 \]

\[ y_7 = 1 \text{ if } (I_2, I_1, I_0) = (1,1,1) \text{ and } En = 1 \]
Decoder Application: universal set \{\text{Decoder, OR}\}

Example: Implement functions $f_1(a,b,c) = \Sigma m(1,2,4)$

$$f_2(a,b,c) = \Sigma m(2,3), \text{ and } f_3(a,b,c) = \Sigma m(0,5,6)$$

with a 3-input decoder and OR gates.
Decoders

• OR minterms

\[ Y = AB + \overline{AB} \]
\[ = A \oplus B \]
Tree of Decoders

Implement a 4-2^4 decoder with 3-2^3 decoders.
Tree of Decoders

Implement a 6-2^6 decoder with 3-2^3 decoders.
2. Encoder

- Definition
- Logic Diagram
- Priority Encoder
A. Any program, circuit or algorithm which encodes
B. In digital audio technology, an encoder is a program that converts an audio WAV file into an MP3 file
C. A device that converts a message from plain text into code
D. A circuit that is used to convert between digital video and analog video
E. All of the above
Encoder Definition: A digital module that converts the assertion of a device to the binary address of the device.

Encoder Description:

At most one $I_i = 1$.

$(y_{n-1}, \ldots, y_0) = i$ if $I_i = 1$ & $En = 1$

$(y_{n-1}, \ldots, y_0) = 0$ otherwise.

$A = 1$ if $En = 1$ and one $i$ s.t. $I_i = 1$

$A = 0$ otherwise.
Encoder: Logic Diagram

I_1 \quad I_3 \quad I_5 \quad I_7 \quad \text{En} \quad y_0

I_2 \quad I_3 \quad I_6 \quad I_7 \quad \text{En} \quad y_1
Encoder: Logic Diagram

\[ \text{Encoder Diagram} \]

\[ \begin{array}{c}
\text{En} \\
\rightarrow \\
\text{y}_2 \\
\end{array} \]

\[ \begin{array}{c}
\text{En} \\
\rightarrow \\
\text{A} \\
\end{array} \]
Priority Encoder: Definition

Description: Input \((I_{2^{n-1}}, \ldots, I_0)\), Output \((y_{n-1}, \ldots, y_0)\)

\[(y_{n-1}, \ldots, y_0) = i \text{ if } I_i = 1 \& En = 1 \& I_k = 0 \text{ for all } k > i \text{ (high bit priority) or}
for all } k < i \text{ (low bit priority).} \]

\[E_o = 1 \text{ if } En = 1 \& I_i = 0 \text{ for all } i, \]
\[G_s = 1 \text{ if } En = 1 \& \exists i \text{ s.t. } I_i = 1. \]

\((G_s \text{ is like } A, \text{ and } E_o \text{ tells us if enable is true or not).}\)
Priority Encoder: Implement a 32-input priority encoder w/ 8 input priority encoders (high bit priority).