CSE140 Exercise 6, No due date

(I) Adders: Design a 4-bit carry-lookahead adder. Show your schematic diagram.

(II) Adders: Follow the topology of the prefix adder schematic in lecture note 14, page 27.

(1) From output 4, we can trace a binary tree that covers input nodes -1 to 3. Repeat the drawing of the binary tree of output 4.

(2) Derive the output expressions for all the nodes of the above binary tree including output 4 (carry bit $C_4$) as a function of inputs $(g_3, p_3, g_2, p_2, g_1, p_1, g_0, p_0, c_{in})$.

(III) System Designs: Implement the following algorithm:

\[
\text{Alg}(X,Y,C,s)\\
\text{Input} \ X[7:0], \ Y[7:0] \ \text{type bit-vector,}\\
\text{s type boolean;}\\
\text{Output} \ C[7:0] \ \text{type bit-vector;}\\
\text{Local-object} \ A[7:0], \ B[7:0] \ \text{type bit-vector;}\\
S1: \ \text{if s' goto S1 else goto S2};\\
S2: \ B \gets X || A \gets Y;\\
S3: \ A \gets \text{Add}(A,B) || \text{if A}[7] \ \text{goto S4 else goto S5};\\
S4: \ A \gets \text{Add}(A,1) || \text{goto S6};\\
S5: \ B \gets \text{Add}(B,1);\\
S6: \ C \gets \text{Add}(A,B) || \text{goto S1};\\
\text{end Alg}
\]

(1) Design a data subsystem that is adequate to execute the algorithm and draw the schematic diagram.

(2) Design a control subsystem and draw the state diagram.

(3) Implement the control subsystem with a one hot encoding design. Draw the logic diagram.

(IV) System Designs: Implement the following algorithm:

\[
\text{Alg}(X,Y,Z,\text{start},U,\text{done})\\
\text{Input} \ X[7:0], \ Y[7:0], \ Z[7:0], \ \text{start;}\\
\text{Output} \ U[7:0], \ \text{done};\\
\text{Local-object} \ A[7:0], \ B[7:0], \ C[7:0];\\
S1: \ \text{If start' goto S1;}\\
S2: \ \text{done \gets 0 || A \gets X || B \gets Y || C \gets Z;}\\
S3: \ A \gets \text{Add}(A,B);\\
S4: \ \text{If B}[7] \ \text{goto S3 || B \gets \text{Inc}(B);}\\
S5: \ \text{If C}[7] \ \text{goto S3 || C \gets \text{Inc}(C);}\\
S6: \ U \gets A || \ \text{done \gets 1 || goto S1;}\\
\text{End Alg}
\]

(1) Design a data subsystem that is adequate to execute the algorithm. Draw the schematic diagram to show the design.

(2) Design the control subsystem (i) draw the state diagram; (ii) draw the logic diagram that implements the control subsystem with a one hot encoding design.