Abstract—In this paper we introduce a 14-core application processor for multimedia mobile applications, implemented in 40 nm, with a 222 mW H.264 full high-definition (full-HD) video engine, a 124 mW 40 M-polygons/s 3D/2D graphics engine, and a video/audio multiprocessor for various Codecs and image processing. The application processor has 25 power domains to achieve coarse-grain power gating for adjusting to the required performance of wide range of multimedia applications. The simple on-chip power switch circuits perform less than 1 µs switching while reducing rush current. Furthermore, the Stacked Chip SoC (SCS) technology enables rewiring to the DRAM chip during assembly/packaging phase using a wire with 10 µm minimum pitch on Re-Distribution Layer (RDL) using electroplating. The peak memory bandwidth is 10.6 GB/s with an x512b SCS-DRAM interface, and the power consumption of this interface is 3.9 mW at 2.4 GB/s workload.

Index Terms—Application processor, full high-definition (full-HD) video, MICRO bump, multiple power domains, on-chip LV-PMOS switch, Re-Distribution Layer (RDL), stacked DRAM.

I. INTRODUCTION

Today’s multimedia mobile devices should support a wide range of multimedia applications in addition to full high-definition (full-HD, 1920 × 1080) video processing. Conventional hardware engine approaches [1]–[4] cannot handle new applications that might be required once the chips have been fabricated. In this paper, we introduce an application processor with a hybrid architecture that combines a hardware based solution by special hardware engines for high performance tasks such as specific full-HD video Codecs and 3-D graphics and a software based solution by a multi-core processor [5], [6] for flexible applications.

Another important issue faced in multimedia mobile devices is to achieve high memory bandwidth with low power consumption. A System-in-Package (SiP) memory interface connection using wire bonding needs a large number of I/Os or high interface frequency at the expense of high power consumption. On the other hand, a Chip-on-Chip (CoC) memory interface connection using micro-bumps is a power-efficient technology to achieve high memory bandwidth and low power consumption [7]. Nonetheless, in the case of conventional CoC technology, because wiring between a logic chip and a DRAM chip is implemented on the metal layers in the DRAM chip, customized DRAM chips are necessary. Furthermore, due to the memory requirements of high resolution video processing, the memory chip area may easily become larger than the logic chip, and in such case, the logic chip should be placed on top of the memory chip. Nonetheless, in such structure the pads of the logic chip can not be connected to the base package by direct wire bonding. Thus, to cope with the above mentioned challenges, we introduce a new Stacked-Chip SoC (SCS) technology that enables rewiring at the assembly/packaging phase by means of a Re-Distribution Layer (RDL).

The recent SoCs for mobile applications support power gating to reduce the power consumption [8], [9]. Our application processor has 25 power domains and controls these domains in accordance to various performance requirements. We also present new on-chip power switches that can adjust the maximum rush current and the recovery time.

This paper is organized as follows. Section II gives an overview of the hybrid application processor for a wide range of multimedia applications that achieved high memory bandwidth with low power consumption. Section III explains the SCS technology using RDL and micro bumps. The multiple power domain control to achieve low power consumption in a wide range of multimedia applications and the measurement results of the multimedia mobile device power consumption are described in Section IV and Section V respectively. Section VI concludes the paper.

II. PROCESSOR OVERVIEW

A. Processor Architecture

We introduce a hybrid architecture that combines a hardware based solution and a software based solution. The hardware engine achieves high performance with low power consumption for specific demanding tasks such as full-HD video and 3D/2D graphics. On the other hand, the software based solution with a multi-core processor supports various multimedia applications such as several video Codecs (H.264, MPEG-4, MPEG-2, and

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VC-1), audio Codecs (MP3, eAAC+ and WMA), image processing tools (frame rate converter and image super resolution) and image recognition tools.

Fig. 1 and Table I show, respectively, the block diagram and the features of the application processor. The chip includes a 435 MHz ARM Cortex-A9 MPCore module, a 333 MHz video/audio multiprocessor, a full-HD video H.264 Codec engine, a 3D/2D graphics engine, an image composition engine, DRAM interfaces, and the I/Os. There are 14 heterogeneous processor cores in total: two ARM processors, eight Media Processing Engines (MPEs) in the video/audio Multiprocessor, two CPU cores in the full-HD video H.264 Codec engine, one CPU core in the TS interface, and one CPU core used as a general controller.

The video/audio multiprocessor supports a variety of multimedia processing applications. The video/audio multiprocessor [5], [6] consists of eight MPEs and a unified 256 KB L2 cache (L2$). Each of these MPEs is a 3-way VLIW customized processor in the video/audio Multiprocessor, two CPU cores in the full-HD video H.264 Codec engine, one CPU core in the TS interface, and one CPU core used as a general controller.

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The video H.264 Codec engine can process up to full-HD (1080i/p) H.264 video by using four 128-bit channels bus interface. The 3D/2D graphics engine supports the OpenGL ES 2.0 specification, and its performance is 40 M-polygons/s and 300 M-pixels/s. Its bus interface has three channels of 128-bit width. The display interface has three types of output paths: to main LCD panel, sub LCD panel and full-HD TV. The camera interface can connect two cameras. These camera and display interfaces have full-HD video input and output capabilities.

The application processor supports two types of external memories, the SCS-DRAM and the DDR-SDRAM. The SCS-DRAM has four 128-bit channels interface and achieves maximum 10.6 GB/s bandwidth at 166 MHz. The SCS-DRAM is used as a video processing memory that requires high data bandwidth. On the other hand, the DDR-SDRAM is used as the main memory of the ARM processors. These separated memory interfaces can reduce memory access latencies and improve the total data bandwidth of the system. Furthermore, the internal data SRAMs in the L2 cache of the video/audio multiprocessor are used as scratch-pad memory of the full-HD video H.264 Codec engine, because the video/audio multiprocessor and the full-HD video H.264 Codec engine execute video Codecs separately and exclusively.

**B. Processor Implementation**

Fig. 2 shows the micrograph of the application processor. The application processor is fabricated in 40 nm CMOS, triple-well,
TABLE I  
FEATURES OF THE APPLICATION PROCESSOR

<table>
<thead>
<tr>
<th>Technology</th>
<th>40 nm CMOS, triple-well,7-layer-metal</th>
</tr>
</thead>
<tbody>
<tr>
<td>Chip size</td>
<td>6.0 mm x 6.2 mm</td>
</tr>
<tr>
<td>Gate counts</td>
<td>18.5 M gates (Logic), 9 M bit (SRAM)</td>
</tr>
<tr>
<td>Supply voltage</td>
<td>1.1 V (core), 1.2 V (PLL), 1.1/1.2/1.5/1.8 V (I/O)</td>
</tr>
<tr>
<td>I/O</td>
<td>651 Ball (Function : 429, VDD/GND : 157, NC : 25, Test : 41)</td>
</tr>
<tr>
<td>Clock frequency</td>
<td>435 MHz(ARM), 400 MHz(HS I/O), 333 MHz(Video/Audio), 255 MHz(H.264 dec.), 166 MHz(Main bus, HS peripheral), 83 MHz(Sub bus, LS peripheral)</td>
</tr>
<tr>
<td>CPU</td>
<td>ARM Cortex™-A9 MPCore™(IS:16 KB, DS:16 KB) x2 Video/Audio MPE 2) x8, H.264 Full-HD Video CPU x2, TS CPU x1, General CPU x1</td>
</tr>
<tr>
<td>Video</td>
<td>H.264 HP 1080i/4i Codec, H.264 BP 720p Codec, MPEG-4 SP FWVGA Codec, MPEG-2 MP@HL Half decoding, VC1 MP QHD decoding, Frame rate converter</td>
</tr>
<tr>
<td>Audio</td>
<td>MP3 / eAAC+ / WMA</td>
</tr>
<tr>
<td>3D/2D Graphics</td>
<td>OpenGL® ES2.0 Pixel Rate :300 M pixel/s(max) (1 texture modulation) Vertex Rate :40 M polygon/s(max) (No lighting)</td>
</tr>
<tr>
<td>External memory I/F</td>
<td>DRAM 128 bits x 4 ch 166 MHz (SCS 1), Mobile-DDR SDRAM 32 bit 166 MHz (SIP)</td>
</tr>
<tr>
<td>Camera I/F</td>
<td>1080p 30 fps(Movie), 24 M pixel (Image)</td>
</tr>
<tr>
<td>Display I/F</td>
<td>Main LCD(720p 60fps 24 bits), Sub LCD(FWVGA 60 fps 24bits), HDMI(1080p 30 fps)</td>
</tr>
<tr>
<td>Other I/F</td>
<td>SD Card I/F, Serial I/O (SPI / I2C) I/F, UART, IR remote I/F, TS I/F, Audio I/F(I2S), Flash memory I/F (NAND/NOR), HS serial (MIPI 3) / TLVDS 4 I/F</td>
</tr>
</tbody>
</table>

1) SCS: Stacked Chip SoC  
2) MPE: Media Processing Engine  
3) MIPI: Mobile Industry Processor Interface  
4) TLVDS: Toshiba Low Voltage Differential Signalling  
OpenGL is a registered trademark of the Silicon Graphics Co..  
Coretex and MPCore are trademarks of the ARM Co..

7-layer metal technology and integrates 18.5 M gates and 9 Mb SRAM on a 6x0 x 6.2 mm² die. The micro bumps for SCS-DRAM interface are located in the middle of the die. The micro bumps are divided into two groups due to limitations in cell placement and wiring and in order to make wiring space for signals between the right side blocks and the left side ones. The analog PLL of the lower right is used for the high speed I/O. The other analog PLLs generate the base clock signals for the ARM

III. STACKED DRAM ARCHITECTURE

A. SCS Technology

The SCS technology connects a logic chip and a memory chip through micro bumps. There are two types of the SCS technology as shown in Fig. 3(a). When memory capacity is relatively small and the memory chip is smaller than the logic chip, the memory chip is placed on top of the logic chip. This structure is the SCS technology type 1, and it allows connecting the
pads of the logic chip to the base package pin by wire bonding. When the memory chip is larger than the logic chip, as the 512 Mb DRAM in our system, the application processor should be placed on top of the memory chip. However, it is not possible to connect the pads of the application processor to the base package directly by wire bonding. That’s why, we have introduced a SCS technology that enables to connect the application processor to the base package using a RDL wiring on the memory chip. This structure is the SCS technology type 2 as shown in Fig. 3(b).

The SCS technology type 2 has an advantage over the type 1 technology because it allows using the same memory chip with different logic chips. This is achieved through the RDL and the micro bumps, even if the chip size, the number of I/Os, and layout are different, as long as the differences in size and layout of the logic chips are adjustable with the RDL. For instance, in Fig. 4, the logic chip (A) is connected to the memory chip through the micro bumps and RDL wiring, and in the same way the logic chip (B) can be connected to the same memory chip. The RDL wiring and micro bumps are able to absorb the differences in the I/Os in the logic chip (A) and (B), during the assembly/packaging phase.

Fig. 5 explains the SCS technology flow. On the memory wafer, 10 μm pitch Cu wiring and 20-μm SnCu micro bumps are formed by electroplating, and then the surface is covered by the protective film. On the logic wafer, only micro bumps are formed. These wafers are diced to form the chips, and then, the memory chip and the logic chip are connected through the micro bumps. The gap between micro bumps is sealed with resin. Fig. 6(a) shows a RDL with minimum 5/5-μm Line/Space and 3-μm thick wires. Fig. 6(b) shows a 20-μm micro bump with 40-μm minimum pitch.

B. Chip Packaging

Fig. 7 shows the stacked DRAM structure of the packaged chip, with two types of memory chips: a SCS-DRAM and a DDR-SDRAM. The SCS-DRAM chip is connected to the application processor with micro bumps. These micro bumps on the SCS-DRAM chip are connected through the RDL. The DDR-SDRAM chip is connected to the application processor through wire bonding, the RDL and the micro bumps. The I/Os of the package are connected to the RDL by wire bonding.
The total power consumption of the packaged chips is up to 660 mW, which causing a maximum temperature rise of 15 degrees in the package. This power consumption number is estimated from the maximum processing performance of the video/audio multiprocessor cores, the ARM processor cores, SCS-DRAM chip and DDR-SDRAM chip. Based on previous products, it is possible to affirm that a temperature rise of up to 15 degrees does not cause problems in the packaged chips.

C. SCS-DRAM Interface Architecture

Fig. 8 shows a schematic diagram of SCS-DRAM interface. In the case of this application processor, the total number of micro bumps connections is 1024 for the 4 channels of 128 bits IO width. The peak memory bandwidth is 10.6 GB/s at 166 MHz. The FIFO buffers have a burst transfer size of 256 bytes. The level shifters are inserted on the boundary of the internal 1.1 V domain and the 1.5 V SCS-DRAM interface. The BIST logic for the SCS-DRAM is included in the application processor. This BIST writes the data to the SCS-DRAM according to test patterns, and then compares the data read from the SCS-DRAM with the expected value. If the comparison fails, an error flag is asserted. Furthermore, the scan flip-flops can test the interface between the SCS-DRAM and the application processor.

D. Power Consumption of SCS-DRAM Interface

The SCS-DRAM interface achieves low power consumption because it uses only 20 μm bumps with about tens of fF capacity and does not require any high drive I/Os nor long wire bonding.

Fig. 9 shows the measured power consumption of one 128-bit SCS-DRAM channel on 1.5 V. We obtain 1 mW at 600 MB/s with maximum workload. The power consumption of four 128-bit SCS-DRAM channels at 2.4 GB/s maximum workload is estimated to be 3.9 mW. Based on the experimental results shown in this graph, the power consumption Y can be described by the following equation where X shows the bit rate of the SCS-DRAM interface:

\[ Y = 1.5842X + 65.434 \] (1)
KIKUCHI et al.: A 40 nm 222 mW H.264 FULL-HD DECODING, 25 POWER DOMAINS, 14-CORE APPLICATION PROCESSOR WITH x512b STACKED DRAM

<table>
<thead>
<tr>
<th>Power Mode</th>
<th>Turn On Domain</th>
<th>Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standby Mode</td>
<td>25</td>
<td>15µW</td>
</tr>
<tr>
<td>Sleep Mode</td>
<td>24, 25</td>
<td>1.7 mW</td>
</tr>
<tr>
<td>All On Mode</td>
<td>1, 2, 3, 4, 5, 6, 7, 8, ... , 24, 25</td>
<td>22 mW</td>
</tr>
</tbody>
</table>

Vdd1 = 1.1 V. Process = cutrix. Temp, = 25°C

Fig. 11. Power supply system.

Table II

<table>
<thead>
<tr>
<th>Power Mode</th>
<th>Turn On Domain</th>
<th>Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standby Mode</td>
<td>25</td>
<td>15µW</td>
</tr>
<tr>
<td>Sleep Mode</td>
<td>24, 25</td>
<td>1.7 mW</td>
</tr>
<tr>
<td>All On Mode</td>
<td>1, 2, 3, 4, 5, 6, 7, 8, ... , 24, 25</td>
<td>22 mW</td>
</tr>
</tbody>
</table>

Vdd1 = 1.1 V. Process = cutrix. Temp, = 25°C

Table II

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<th>Power</th>
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<td>24, 25</td>
<td>1.7 mW</td>
</tr>
<tr>
<td>All On Mode</td>
<td>1, 2, 3, 4, 5, 6, 7, 8, ... , 24, 25</td>
<td>22 mW</td>
</tr>
</tbody>
</table>

Vdd1 = 1.1 V. Process = cutrix. Temp, = 25°C

B. On-Chip Switch Architecture

Fig. 12 shows the schematic diagram of the on-chip switch controller. The on-chip power switch scheme utilizes two types of pMOS transistors, named TP1 and TP2, with different channel widths. The switch cell named U1 has a coupling capacitor named C1 between the gate node of the TP1 and a virtual VDD, VDDV, but the switch cell named U2 does not have the capacitor. When the number of U1 cells is reduced in the power domain, the total coupling capacity decreases and the maximum rush current increases. On the other hand, when there are many U1 cells in the power domain the total coupling capacity increases and the maximum rush current decreases, but the area overhead and the recovery time become large. The transistors TN1 in the buffer cell B1 adjust the driving force, and introduce a trade-off between the recovery time and the maximum rush current. Thus, the on-chip power switch architecture can adjust the maximum rush current and the recovery time by the number of U1 switch cells and the structure of the buffer cell B1.

Fig. 13 shows the switch layout and the power domain control flow. In some implementation cases, the switch cells can be placed evenly in all over the power domain, but in our implementation the switch cells U1 and U2 are placed on the upper and lower edges of the power domain to make the physical design easier. The on-chip switch controller in Fig. 13 operates as follows. First the power enable signal becomes active from the B1, and the TP1 switches in U1 and U2 cells are turned on 10% of the power supply. Then, the TP2 switches in U1 and U2 cells are turned on completely (100%). The channel width of TP1 is 10 µm, and the channel width of TP2 is 90 µm.

A rush current might be generated at an instant when the power switch is turned on to activate a power domain. If a rush current occurs, a power line voltage of the external power source varies, and the power supply to another activated power domain becomes unstable, which might cause the logic circuit in the power domain to malfunction. This might consequently cause a problem/multifunction in the application processor. For example, supposing that when a user is listening to a song, he wants to watch the video clip of it, the audio and the video should be synchronized and the video decoder domain should be turned on while the audio decoder domain is under operation. Fig. 14 shows the maximum rush current (up to 20 mA) and the maximum recovery time (within 1 s) under worst-case conditions. The rush current and recovery time depend on the inclination and form of PC1, which depends on the number of U1 cell and TN1 transistor. The required performance for coarse-grain power gating is achieved at this rush current and recovery time.

The design with multiple power domains requires a large number of switches, but as the area of the switches increases it becomes a major overhead. We have developed the on-chip switches that are simple and small. The total area of this chip’s on-chip switches is 0.927 mm². This area accounts for 2.5% of the application processor (37.2 mm²). The total leakage power consumption of on-chip switches is 10 µW. The leakage power...
TABLE III
MEASUREMENT RESULTS OF CHIP POWER CONSUMPTION BY HW SOLUTION

<table>
<thead>
<tr>
<th>Application</th>
<th>Scenario</th>
<th>Resolution</th>
<th>Frame Rate</th>
<th>Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>H.264</td>
<td>High Profile Decoding</td>
<td>1920x1080</td>
<td>30 fps</td>
<td>222 mW</td>
</tr>
<tr>
<td></td>
<td></td>
<td>640x480</td>
<td>15 fps</td>
<td>71 mW</td>
</tr>
<tr>
<td></td>
<td>High Profile Encoding</td>
<td>1920x1080</td>
<td>10 fps</td>
<td>232 mW</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1280x720</td>
<td>30 fps</td>
<td>132 mW</td>
</tr>
<tr>
<td>3D</td>
<td>OpenGL® ES2.0</td>
<td>40 M polygon/s</td>
<td></td>
<td>124 mW</td>
</tr>
</tbody>
</table>

Vdd = 1.1 V, Process = center, Temp, = 25°C

TABLE IV
MEASUREMENT RESULTS OF CHIP POWER CONSUMPTION BY SW SOLUTION

<table>
<thead>
<tr>
<th>Application</th>
<th>Scenario</th>
<th>Audio Option</th>
<th>Resolution</th>
<th>Frame Rate</th>
<th>Number of Active MPE</th>
<th>Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPEG-4</td>
<td>Simple Profile Dec.</td>
<td>None</td>
<td>640x480</td>
<td>15 fps</td>
<td>7 MPEs</td>
<td>79 mW</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AAC Dec. 48 kHz 256 kbps stereo x 2</td>
<td>854x480x2</td>
<td>30 fps</td>
<td>8 MPEs</td>
<td>237 mW</td>
</tr>
<tr>
<td></td>
<td>Main Profile at High Level Dec.</td>
<td>None</td>
<td>960x1080</td>
<td>30 fps</td>
<td>8 MPEs</td>
<td>249 mW</td>
</tr>
<tr>
<td></td>
<td>Simple Profile Enc.</td>
<td>None</td>
<td>320x240</td>
<td>15 fps</td>
<td>7 MPEs</td>
<td>72 mW</td>
</tr>
<tr>
<td>H.264</td>
<td>Baseline Profile Dec.</td>
<td>None</td>
<td>320x240</td>
<td>15 fps</td>
<td>3 MPEs</td>
<td>37 mW</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AAC Dec. 48 kHz 128 kbps stereo</td>
<td>320x240</td>
<td>15 fps</td>
<td>3 MPEs</td>
<td>42 mW</td>
</tr>
<tr>
<td></td>
<td>High Profile Dec.</td>
<td>None</td>
<td>640x480</td>
<td>15 fps</td>
<td>2 MPEs</td>
<td>70 mW</td>
</tr>
<tr>
<td></td>
<td>Baseline Profile Enc.</td>
<td>AAC Enc. 48 kHz 64 kbps stereo</td>
<td>320x240</td>
<td>15 fps</td>
<td>7 MPEs</td>
<td>79 mW</td>
</tr>
<tr>
<td></td>
<td></td>
<td>None</td>
<td>854x480</td>
<td>30 fps</td>
<td>8 MPEs</td>
<td>315 mW</td>
</tr>
</tbody>
</table>

Vdd = 1.1 V, Process = center, Temp, = 25°C

Fig. 14. Maximum rush current and recovery time.

consumption accounts for only 0.6% of the application processor (1.7 mW).

V. POWER CONSUMPTION RESULTS

Table III shows the measurement results of the chip power consumption by the hardware based solution. Fig. 15 shows the comparison with previous work [1], [4]. The power consumption of the H.264 1920 × 1080 30 fps decoding when using the full-HD H.264 Codec engine is 222 mW, and the power consumption of the H.264 1280 × 720 30 fps encoding when using the Codec engine is 132 mW. The power consumption is less than that of the hardware engine in ISSCC2009 [1], because our Codec engine is simple and only designed for H.264 in addition to process technology improvement. When comparing our result with the software multi-core processor implementation in ISSCC2008 [5], our hardware solution achieves lower power consumption at high performance such as H.264 1280 × 720 30 fps encoding.

Table IV shows the measured chip power consumption for a software based solution. The video/audio multiprocessor
achieves the same degree of power consumption as the full-HD H.264 Codec engine but at a lower video processing performance, such as a H.264 VGA 15 fps decoding with only two active MPEs. The power consumption of the full-HD H.264 Codec engine can not be reduced because the hardware engine uses many high-speed cells and it is designed to achieve high performance.

Fig. 16 shows the evaluation board of the application processor, which can be used to measure the power consumption in real time. The evaluation board has an LCD panel, a camera, a microphone, a speaker and an SD card slot.

VI. CONCLUSIONS

We have developed a hybrid application processor that combines a hardware based solution and a software based solution. The hardware based solution achieves H.264 1080p decoding with 222 mW. The 3D/2D graphics performance is 40 M-polygons/s and 300 M-pixels/s. The software based solution achieves the same degree of low power as the hardware based solution by 25 power domain control at H.264 VGA 15 fps decoding. The peak memory bandwidth of the SCS-DRAM interface is 10.6 GB/s and RDL minimum L/S is 5/5 μm. 23 of the 25 power domains on the chip has controllable. Total leakage power by multiple power domain control is 1.7 mW at sleep mode. The maximum rush current of each power domain is 20 mA and the maximum recovery time is within 1 μs under worst-case conditions.

REFERENCES


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Mr. Koshio is a member of Japan Electronics and Information Technology Industries Association, Technical Committee on Semiconductor Packaging, Sub-Committee on Integrated Circuits Package, and Sub-Committee on General Rules and Common.}

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