SATURNINO GARCIA

Computer Science & Engineering Department

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RESEARCH INTERESTS:

My research interests lie in the areas of compilers, program analysis, and parallel software engineering. My current research involves creating automated tools to increase the efficiency of parallel programmers and reduce the risk of parallel software development. I also have an active interest in computer science education research.

EDUCATION:

University of California, San Diego

Ph.D. in Computer Science   Expected: 2012
Thesis: Compiler Support for Multicore Parallel Programming
Advisor: Michael B. Taylor

C.Phil. in Computer Science   2010
M.S. in Computer Science   2007

Drexel University

B.S. in Computer Engineering, Minor in Philosophy   2005
Highest overall GPA in College of Engineering.

TEACHING EXPERIENCE:

Instructor, *University of California, San Diego*
Response rates to "Do you recommend this professor?" are given with each course. Full course evaluation results are available at http://www.cape.ucsd.edu

Introduction to Computer Architecture (CSE 141)
Summer 2011. (100% recommended in evaluations)

Project in Computer Architecture (CSE 141L)
Summer 2011 (90% recommended in evaluations)

Master Teaching Assistant, *University of California, San Diego*
  Currently serving (2011-12) as Master TA for Computer Science and Engineering Department.
  Tasks include: serving as TA for "Teaching Methods in Computer Science" course, serving as a
  liason between TAs and department, and mentoring new TAs.

Teaching Assistant, *University of California, San Diego*
  Consistantly rated among the top TA's with an average evaluation score of 4.5 out of 5. (Individual
  scores are given beside quarter, if available.) Mentored junior TA's through "Teaching Methods in
  Computer Science" course. Selected to speak to UCSD's Council on Educational Policy as part of
  2011 CSE undergraduate program review.

  Project in Computer Architecture (CSE 141L)
    Spring 2011 (4.51), Fall 2008 (Score: 4.71), Spring 2008 (Score: 4.76)

  Principles of Computer Operating Systems (CSE 120)
    Summer 2008

  Discrete Mathematics (CSE 20)
    Summer 2008

  Intro to Computer Architecture (CSE 141)
    Winter 2008 (Score: 4.38), Summer 2007, Spring 2007 (Score: 4.34), Winter 2007 (Score: 4.50)

  Graduate Computer Architecture (CSE 240A)
    Fall 2007 (Score: 4.33), Fall 2006 (Score: 4.50)

  Components and Design Techniques for Digital Systems (CSE 140)
    Summer 2007

Teaching Assistant, *Drexel University*
  Systems II (TDEC 222)
    Summer 2004

Honors & Awards:

Alliance for Graduate Education and the Professoriate Fellowship   2005
  University of California, San Diego
  Awarded to outstanding underrepresented minorities in science, engineering, and math
  doctoral programs with a commitment to support student diversity issues and activities
  at UCSD.

Irwin and Joan Jacobs Fellowship   2005 - 2008
  University of California, San Diego
  Highest honor available to graduate students in the Jacobs School of Engineering.
  Based on academic achievement, leadership, and commitment to community.

Best Poster Award, Computer Science & Engineering 2011
Jacobs Research Expo, University of California, San Diego

Best Student Poster Award 2011
Principles and Practices of Parallel Programming (PPoPP)

Milton Rosenberg Scholarship 2005
Drexel University
Awarded to one outstanding engineering student for academic achievement through their Junior year.

I. Ray Dunlap Scholarship 2004, 2003
Drexel University
Presented to engineering students of high academic achievement, worthiness, and need.

Boeing Engineering Award 2003
Drexel University
Awarded to an undergraduate student in Computer Science recognizing academic contributions.

Arthur and Blanche Garroway Vanaman Scholarship 2002
Drexel University
Awarded to an undergraduate student in recognition of academic achievement.

PROFESSIONAL EXPERIENCE:

Graduate Research Assistant, *University of California, San Diego* 2008 – Present
Advised by: Michael B. Taylor

Lead researcher on Kremlin project, which significantly reduces the effort required to parallelize programs by answering the question, "What parts of my program should I spent time parallelizing?" Led implementation and maintenance of dynamic analysis infracture. Led user study involving graduate parallel architecture course at UCSD. Mentored undergraduate researcher for several years on the project.

Provided LLVM compiler expertise to several other research groups including the Arsenal/GreenDroid project, secure embedded processors, and simultaneous multi-threading group. Created and maintained infrastructure for automatically identifying and refactoring code suitable for conversion to specialized hardware in the Arsenal project.

Graduate Research Assistant, *University of California, San Diego* 2005 – 2008
Advised by: Alex Orailoglu

Researched methods for increasing the reliability of nanoelectronic architectures. These emerging architectures offer the potential for continuing Moore's Law past the end of CMOS scaling but face daunting reliability challenges. I developed low-cost ways of increasing the fault-tolerence of these systems.

Undergraduate Research Assistant, *Drexel University*   2003 – 2005
Advised by: Moshe Kam and William Regli

> Researched secure wireless ad-hoc networks as a member of the "Secure Wireless Agent Testbed" (SWAT) group.

Control Systems Engineering Intern, *Honeywell, Inc.*   2002

> Oversaw regular regression testing of control system software. Worked as member of quality assurance team, testing software updates before they were released to customers.

LEADERSHIP ACTIVITIES:

Coordinator   2007 – 2010
CSE Graduate Student Association, *University of California, San Diego*

> Coordinated computer science graduate student activities such as faculty recruitment, graduate student admissions, and social events.

Founding Member, Academic Committee Chair   2007 – 2011
Jacobs Graduate Student Council, *University of California, San Diego*

> Helped draft organization's constitution. Chaired academic committee, having organized events such as the bi-annual research symposium and the annual Jacobs Research Expo networking reception.

PUBLICATIONS:

All publications are available for download from my website: http://cseweb.ucsd.edu/~s4garcia

Peer-reviewed Journal Articles

> **The GreenDroid Mobile Application Processor: An Architecture for Silicon's Dark Future**. N. Goulding-Hotta, J. Sampson, G. Venkatesh, S. Garcia, J. Auricchio, P.C. Huang, M. Arora, S. Nath, V. Bhatt, J. Babb, S. Swanson, M.B. Taylor. *IEEE Micro Magazine*, March-April 2011.

Refereed Conferences

> **Kismet: Parallel Speedup Estimates for Serial Programs.** D. Jeon, S. Garcia, C. Louie, M.B. Taylor. *Object Oriented Programming Systems Languages and Applications (OOPSLA) 2011.*

> **Kremlin: Rethinking and Rebooting gprof for the Multicore Age**. S. Garcia, D. Jeon, C. Louie, M.B. Taylor. *Programming Language Design and Implementation (PLDI) 2011.*

Kremlin: like gprof, but for parallelization. D. Jeon, <u>S. Garcia</u>, C. Louie, S. Kota Venkata, M.B. Taylor. *Principles and Practices of Parallel Programming (PPoPP) 2011*. *Received "Best Student Poster" Award.*

Efficient Complex Operators for Irregular Codes. J. Sampson, G. Venkatesh, N. Goulding-Hotta, <u>S. Garcia</u>, S. Swanson, M.B. Taylor. *International Symposium on High-Performance Computer Architecture (HPCA) 2011.*

Conservation Cores: Reducing the Energy of Mature Computations. G. Vankatesh, J. Sampson, N. Goulding, <u>S. Garcia</u>, V. Bryksin, J. Lugo-Martinez, S. Swanson, M.B. Taylor. *Architectural Support for Programming Languages and Operating Systems (ASPLOS) 2010.*

SD-VBS: The San Diego Vision Benchmark Suite. S. Kota Venkata, I. Ahn, D. Jeon, A. Gupta, C. Louie, <u>S. Garcia</u>, S. Belongie, and M.B. Taylor. *IEEE Interational Symposium on Workload Characterization (IISWC) 2009.*

Making DNA Self-Assembly Error Proof: Attaining Small Growth Error Rates Through Embedded Information Redundancy. <u>S. Garcia</u> and A. Orailoglu. *Design, Automation, and Test in Europe (DATE) 2009.*

Online Test and Fault-Tolerance for Nanoelectronic Programmable Logic Arrays. <u>S. Garcia</u> and A. Orailoglu. *International Symposium on Nanoelectronic Architectures (NANOARCH) 2008.*

Refereed Workshops

Parkour: Parallel Speedup Estimates for Serial Programs. D. Jeon, <u>S. Garcia</u>, C. Louie, M.B. Taylor. *USENIX Workshop on Hot Topics in Parallelism (HotPar) 2011.*

Bridging the Parallelization Gap: Automating Parallelism Discovery and Planning. <u>S. Garcia</u>, D. Jeon, C. Louie, S. Kota Venkata, M.B. Taylor. *USENIX Workshop on Hot Topics in Parallelism (HotPar) 2010.*

A Secure Wireless Agent-based Testbed. G. Anderson, L. Urbano, G. Naik, D. Dorsey, A. Mroczkowski, D. Artz, N. Morizio, A. Burnheimer, K. Malfettone, D. Lapadat, E. Sultanik, <u>S. Garcia</u>, M. Peysakhov, W.C. Regli, M. Kam. *International Workshop on Information Assurance (IWIA) 2004.*

REFERENCES:

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Dr. Beth Simon
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Lecturer with Security of Employment, Computer Science & Engineering
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