1) Sequential logic implementation

Consider the following incompletely-specified Mealy machine ("**" indicates don’t cares).

Suppose we use the following state encoding. (Assume the name the input variable is $I$.)

<table>
<thead>
<tr>
<th>State</th>
<th>$S_2S_1S_0$</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>100</td>
</tr>
<tr>
<td>B</td>
<td>010</td>
</tr>
<tr>
<td>C</td>
<td>001</td>
</tr>
</tbody>
</table>

Derive the minimum two-level logic for each of the following (you should minimize each logic function separately, no need to worry about sharing logic between logic functions).

\[
\begin{align*}
F &= \\
S_2^+ &= \\
S_1^+ &= \\
S_0^+ &= 
\end{align*}
\]
2) Datapath/registers

Consider the following diagram.

Given the values for control input $S$, the data inputs $X_3X_2X_1X_0$, and the flip-flop values $P_3P_2P_1P_0$ and $Q_3Q_2Q_1Q_0$, what will be the new flip flop values $P_{3}^{+}P_{2}^{+}P_{1}^{+}P_{0}^{+}$ and $Q_{3}^{+}Q_{2}^{+}Q_{1}^{+}Q_{0}^{+}$?

Note: All MUXes are controlled by the same control input $S$, and 0 and 1 mean a constant logic value of “false” ("0") and “true” ("1"), respectively.

<table>
<thead>
<tr>
<th>$S$</th>
<th>$X_3X_2X_1X_0$</th>
<th>$P_3P_2P_1P_0$</th>
<th>$Q_3Q_2Q_1Q_0$</th>
<th>$P_{3}^{+}P_{2}^{+}P_{1}^{+}P_{0}^{+}$</th>
<th>$Q_{3}^{+}Q_{2}^{+}Q_{1}^{+}Q_{0}^{+}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0000</td>
<td>0100</td>
<td>1111</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>1101</td>
<td>1110</td>
<td>0011</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0111</td>
<td>1010</td>
<td>1101</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1000</td>
<td>0000</td>
<td>1011</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
3) Timing analysis

Consider the following sequential logic diagram.

Assume the gate delay is 2 ns for both 2-AND and 2-OR. Assume the positive edge-triggered flip-flop delay is \( T_{\text{delay} FF} = 1 \) ns, and assume the positive edge-triggered flip-flop setup time is also \( T_{\text{setup} FF} = 1 \) ns.

Fill out the rest of the timing diagram for \( A, B, C, D \), and \( E \).
4) Clock period analysis

Consider the following sequential logic diagram where $A$, $B$, $C$, and $D$ are external inputs.

Assume the gate delay for 2-AND is 2 ns, assume the positive edge-trigged flip-flop delay is $T_{delay_{FF}} =$ 1 ns, and assume the positive edge-trigged flip-flop setup time is also $T_{setup_{FF}} =$ 1 ns.

What is the minimum clock period that would satisfy these delays? Provide the critical path.

Clock period =

Critical path =
5) Reverse engineer sequential circuit to finite state machine

\[ F = S_2^+ + S_1^+ + S_0^+ \]

b) Assume initial state is 000, fill in the following state table. If a state is not reachable, indicate the appropriate don’t cares (use "*" to indicate don’t cares).

\[
\begin{array}{c|c|c|c|c}
S_2S_1S_0 & S_2^+S_1^+S_0^+ & \text{ } & \text{ } & F \\
\hline
000 & \text{ } & \text{ } & \text{ } & \text{ } \\
001 & \text{ } & \text{ } & \text{ } & \text{ } \\
010 & \text{ } & \text{ } & \text{ } & \text{ } \\
011 & \text{ } & \text{ } & \text{ } & \text{ } \\
100 & \text{ } & \text{ } & \text{ } & \text{ } \\
101 & \text{ } & \text{ } & \text{ } & \text{ } \\
110 & \text{ } & \text{ } & \text{ } & \text{ } \\
111 & \text{ } & \text{ } & \text{ } & \text{ } \\
\end{array}
\]

c) With initial state = 000, what states, if any, are not reachable?