1) Number representation

a) Represent these numbers in 6-bit signed 2’s complement form or indicate that it is not possible.

<table>
<thead>
<tr>
<th>Number</th>
<th>6-bit Signed 2’s Complement</th>
</tr>
</thead>
<tbody>
<tr>
<td>-1</td>
<td></td>
</tr>
<tr>
<td>-7</td>
<td></td>
</tr>
<tr>
<td>63</td>
<td></td>
</tr>
<tr>
<td>-5</td>
<td></td>
</tr>
<tr>
<td>34</td>
<td></td>
</tr>
<tr>
<td>-32</td>
<td></td>
</tr>
</tbody>
</table>

b) For each binary vector below, what does it represent in Octal and Hexadecimal?

<table>
<thead>
<tr>
<th>Binary</th>
<th>Octal</th>
<th>Hexadecimal</th>
</tr>
</thead>
<tbody>
<tr>
<td>101111</td>
<td></td>
<td></td>
</tr>
<tr>
<td>110000</td>
<td></td>
<td></td>
</tr>
<tr>
<td>011110</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
2) Two-level logic minimization

\[ F(A, B, C, D) = \sum m(1, 6, 7, 10, 11, 12, 13) \]
\[ d(A, B, C, D) = \sum m(0, 3, 5, 9, 15) \]

\[
\begin{array}{cccc}
\text{CD} & 00 & 01 & 11 & 10 \\
\text{AB} & \\
00 & \\
01 & \\
11 & \\
10 & \\
\end{array}
\]

a) Identify all the prime and essential prime implicants.

<table>
<thead>
<tr>
<th>Primes (including Essentials)</th>
<th>Essential Primes Only</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>

b) Find the minimum two-level logic implementation.

\[ F = \]
3) Multi-level logic minimization

Given following logic equations, minimize the number of literals, e.g. by using common subexpressions, Boolean rules, etc. You can introduce new immediate equations for common sub-expressions if it helps to reduce the number of literals. Put a box around your final answer, and indicate the number of literals in your final answer.

\[
\begin{align*}
P &= (\bar{A} + \bar{B} + \bar{C})(D + C + \bar{C}) \\
Q &= ABC\bar{D} + ABC\bar{E} + ABC\bar{F} \\
R &= \bar{B}DEF + CDEF + DEF \\
S &= A\bar{B}(\bar{A} + B) \\
T &= DEF + (\bar{A} + \bar{B} + \bar{C})(\bar{D} + \bar{E} + \bar{F})
\end{align*}
\]
4) Delay analysis

Consider the following 8-bit Carry Select Adder design that adds the numbers $F = X + Y$. Assume 1ns gate delay for all gates (i.e., 2-XOR, 2-AND, 2-OR, and 2-input MUX).

What are final delays for the following:

- $S_0 = \ldots$
- $S_1 = \ldots$
- $S_2 = \ldots$
- $S_3 = \ldots$
- $S_4 = \ldots$
- $S_5 = \ldots$
- $S_6 = \ldots$
- $S_7 = \ldots$
- $C_8 = \ldots$

The logic for each bitslice (rectangle box) is as follows: