1) Sequential logic implementation

Consider the following incompletely-specified Mealy machine ("**" indicates don’t cares).

Suppose we use the following state encoding. (Assume the name the input variable is \( I \).)

<table>
<thead>
<tr>
<th>State</th>
<th>( S_1S_0 )</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>00</td>
</tr>
<tr>
<td>B</td>
<td>10</td>
</tr>
<tr>
<td>C</td>
<td>01</td>
</tr>
</tbody>
</table>

Derive the minimum two-level logic for each of the following (you should minimize each logic function separately, no need to worry about sharing logic between logic functions).

\[
F = \overline{S_1} \\
S_1^+ = \overline{I} \\
S_0^+ = IS_1
\]
2) Timing analysis

Consider the following sequential logic diagram.

Assume the gate delays are 2 ns for 2-AND and 2-OR gates and 1 ns for inverters. Assume the positive edge-trigged flip-flop delay is $T_{delay_{FF}} = 1$ ns, and setup time is also $T_{setup_{FF}} = 1$ ns.

Fill out the rest of the timing diagram for $A$, $B$, $C$, $D$, $E$, $F$, and $G$. 
3) Clock period analysis

Consider the following sequential logic diagram where $A$ and $B$ are external inputs.

Assume the gate delay is 2 ns for a 2-AND gate and 3 ns for a 2-XOR gate. Assume the positive edge-trigged flip-flop delay is $T_{\text{delay}_{FF}} = 1$ ns, and setup time is also $T_{\text{setup}_{FF}} = 1$ ns.

What is the minimum clock period that would satisfy these delays? Provide the critical path.

Clock period = 15 ns

Critical path = F or $L \rightarrow G \rightarrow H \rightarrow K \rightarrow J \rightarrow C$
4) Reverse engineer sequential circuit to finite state machine

![Sequential Circuit Diagram]

a) Fill out the following functions.

\[
F = I + S_1 S_2 + S_0 = S_2^+ + S_0 = S_1^+ + S_0 \\
S_2^+ = I + S_1 S_2 \\
S_1^+ = I + S_1 S_2 = S_2^+ \\
S_0^+ = I + S_0
\]

b) Assume initial state is \textbf{000}, draw the state diagram. **Important:** Only include reachable states in the diagram.

![State Diagram]

c) With initial state = \textbf{000}, what states, if any, are not reachable?

001, 010, 011, 100, 101, 110