

CSE 141L

Steven Swanson
Vasileios Kontorinis

**You will design and
implement a
microprocessor this
quarter!**

Course Goals

- Apply what you learned in 141
 - See architecture play itself out in a real design
 - Learn (more) Verilog
 - Get experience working on a large-scale project
 - Have Fun!
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- “I hear, I forget. I see, I remember. I do, I understand.”

Course Format

- Six labs
 - More about these in a moment.
- Lectures
 - Verilog coding
 - Discuss current or upcoming lab
 - Work through part of the lab
 - Answer questions about the lab
 - Sort of like group office hours
- On November 25th, in place of normal class, we will practice our independent study, learning, and hacking skills.

Lab 1: Introduction Xilinx ISE

- 1 week
- Two Xilinx tutorials
 - Building projects
 - Entering verilog
 - Simulation
 - etc.
- Build, simulate, and synthesize simple circuits
- Measure their properties
- These are skills you will need throughout the class
- Start now!

Lab 3: Simple Control

- 1 week.
- Add control the datapath in Lab 2
- Execute simple programs
- You have now built a simple processor! But not a very useful one.

Lab 4: Your own datapath

- 2 weeks
- Use an ISA from cse141
- Design and implement the datapath needed to execute the instructions.
- Design review with another team.

Lab 5: Control for your processor

- 2 weeks
- Implement the control path for your processor
- You will now have a working CPU! Hurrah!
- Evaluate the performance of your CPU with some simple benchmarks.

Lab 6: Make your CPU Cooler

- 2-3 weeks
- The sky is the limit
 - Pipelining
 - Build a multiprocessor
 - Branch prediction
 - Speculation
 - Multi-media instructions
 - ???

Link to I4I

- You do not need to be in I4I to take I4IL
- We will use the results of the I4I project in this class
 - I4I Project: Design a 17-bit instruction, 34-bit data ISA
 - Due just before the start of Lab 3.
- If you are not in I4I, you will “license” an ISA from one of the groups in I4I
 - License is free to you. The licensor gets extra credit.

Doing the work

- Lab 1 will be done independently
- Lab 2-6 will be in groups of 2-3
 - Higher standards for groups of 3
 - Regrouping is allowed for labs 4-6
 - Choose your groups carefully
 - If your group breaks up at after lab 4 begins, you are stuck.
- The overarching philosophy is “learn by doing”
 - You (and your group) must do all your own coding and design.
 - *You should absolutely talk to other students in the class about Xilinx problems, design options, etc.*
 - Labs 1-3 are specifically for this: you are all building the same thing. Learn from each other!

Lab space and Software

- We will use the Xilinx tools for development
 - Verilog entry
 - Simulation
 - Debugging facilities
 - Like *all* hardware design tools, there are bugs.
 - These are among the best tools available, hard as that may be to believe.
- The labs in the CSE basement have the tools installed
- They are also available for free (see link on the website)
 - **YOU MUST GET VERSION 10.1 AND INSTALL ALL THE PATCHES!!! The current version is 11. We are not using 11.**

Course Staff

- Prof: Steven Swanson
- TA: Vasileios Kontorinis
- One of us will be in the lab 2 nights per week.
 - We hate to be lonely!
 - We will fix the room and time shortly.
- See course web site for details.



Grading

- Two grading schemes
- By the numbers
 - Six labs + class participation
 - ~Equal weight on each (14% per lab, 16% participation)
- Outcome-based
 - Do a reasonable job on the labs (at least a C)
 - Deliver a working processor.
 - You get an A.