

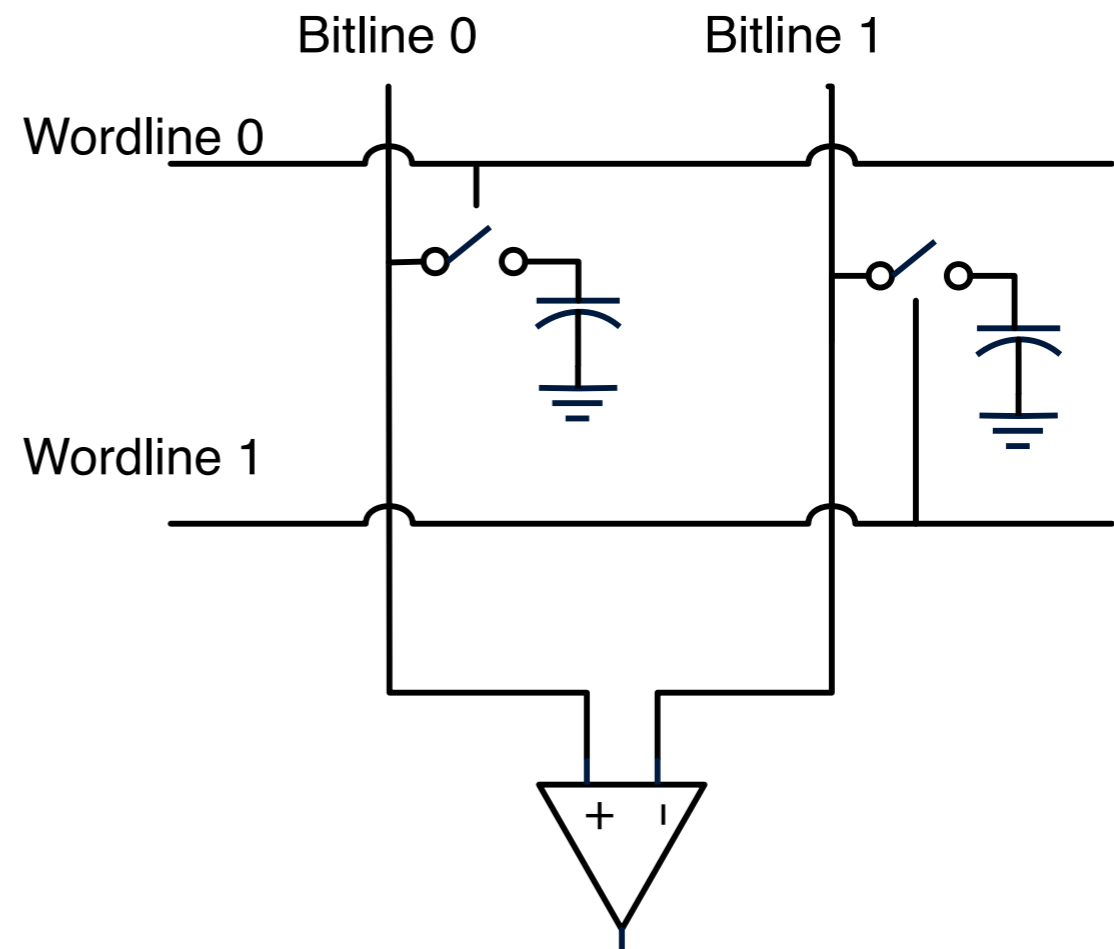
**DRAM**

# Dynamic Random Access Memory (DRAM)

- **Storage**
  - Charge on a capacitor
  - Decays over time (us-scale)
  - This is the “dynamic” part.
  - About  $6F^2$ : 20x better than SRAM
- **Reading**
  - Precharge
  - Assert word line
  - Sense output
  - Refresh data

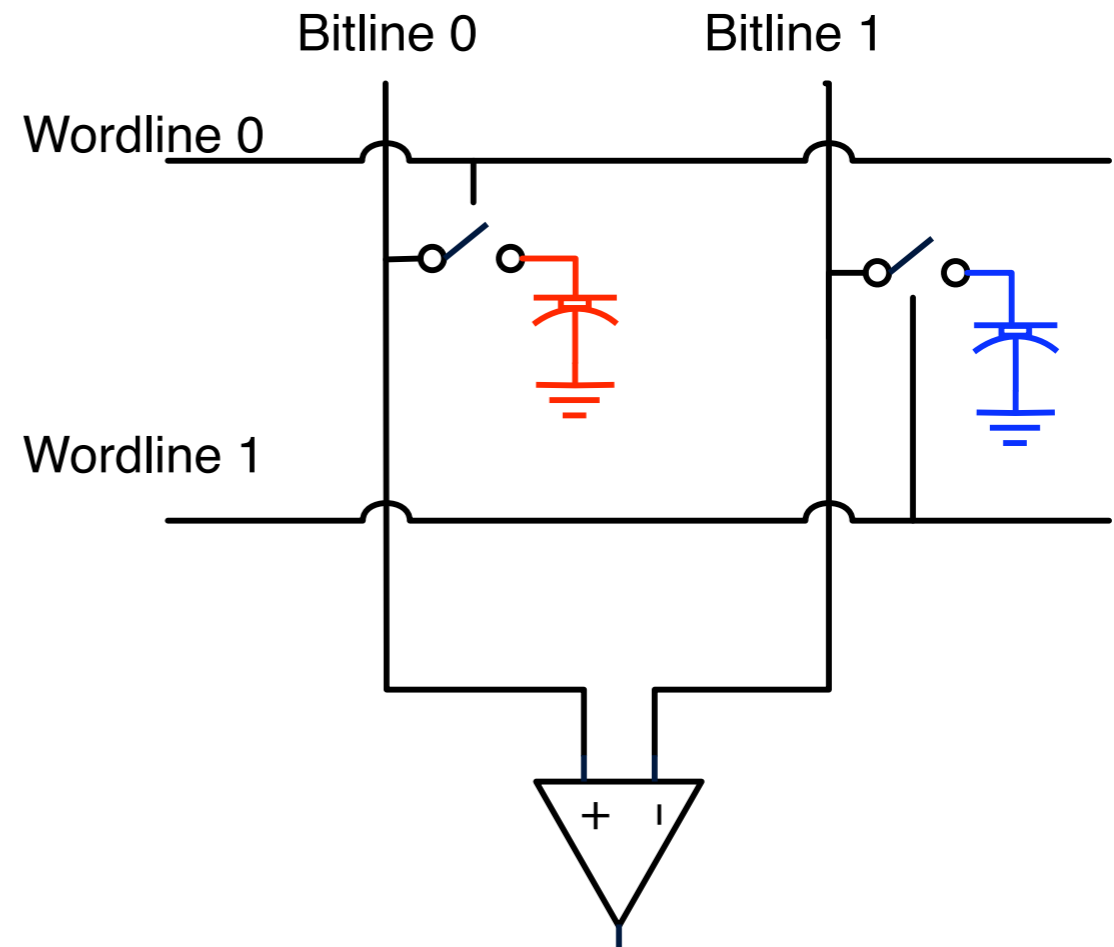
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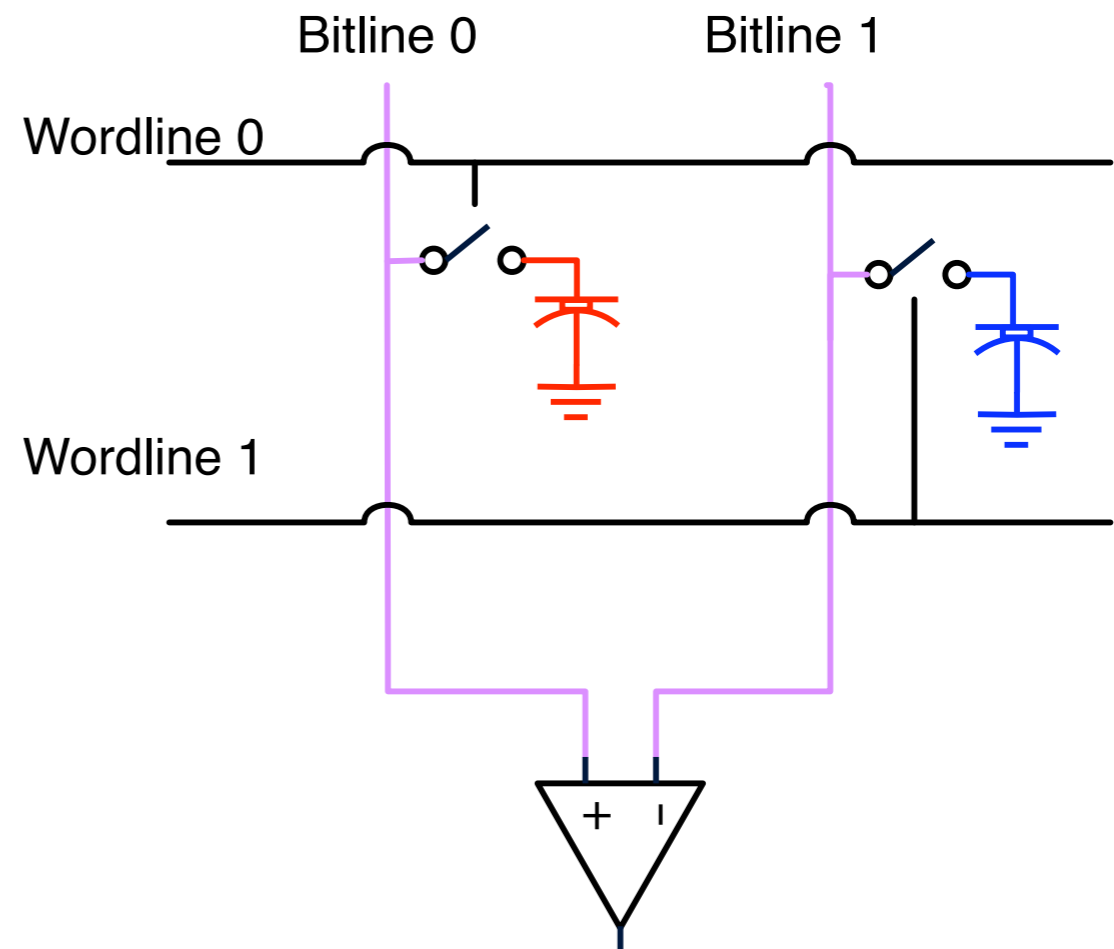
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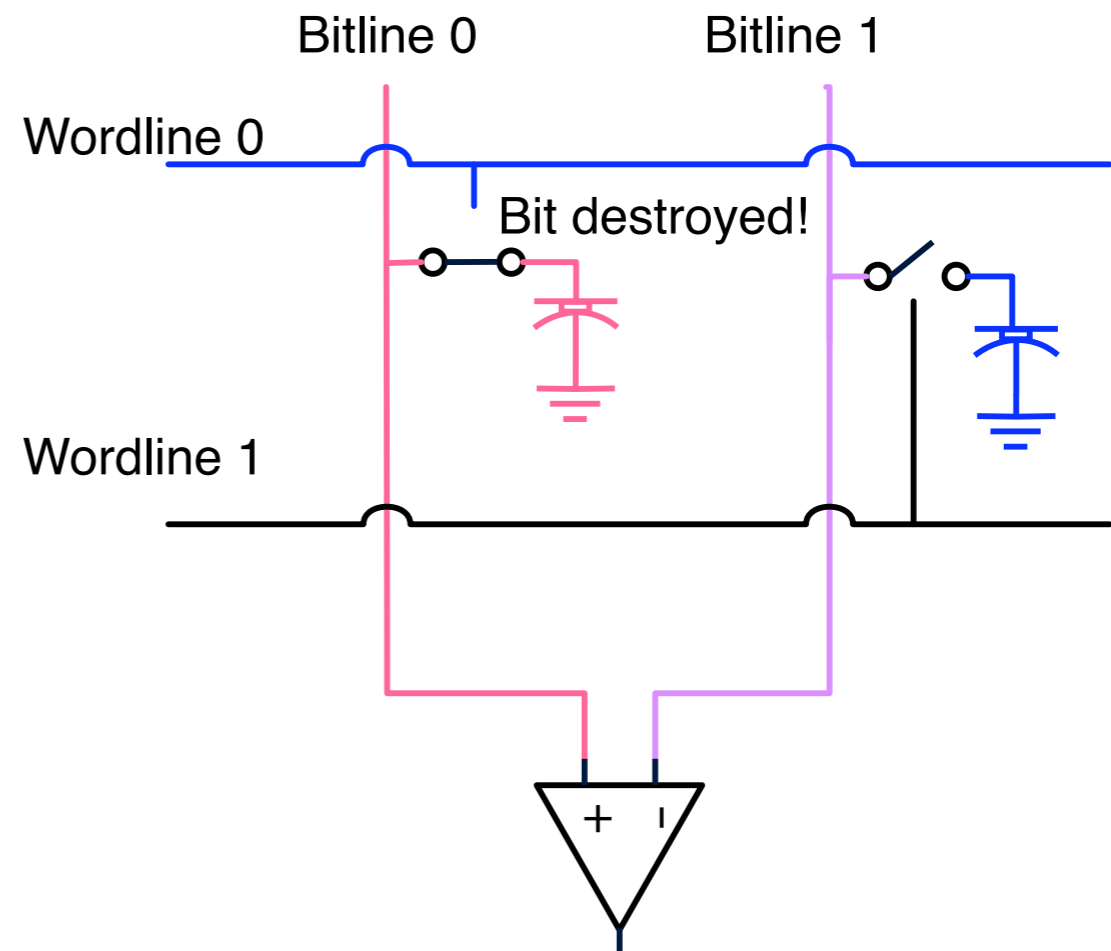
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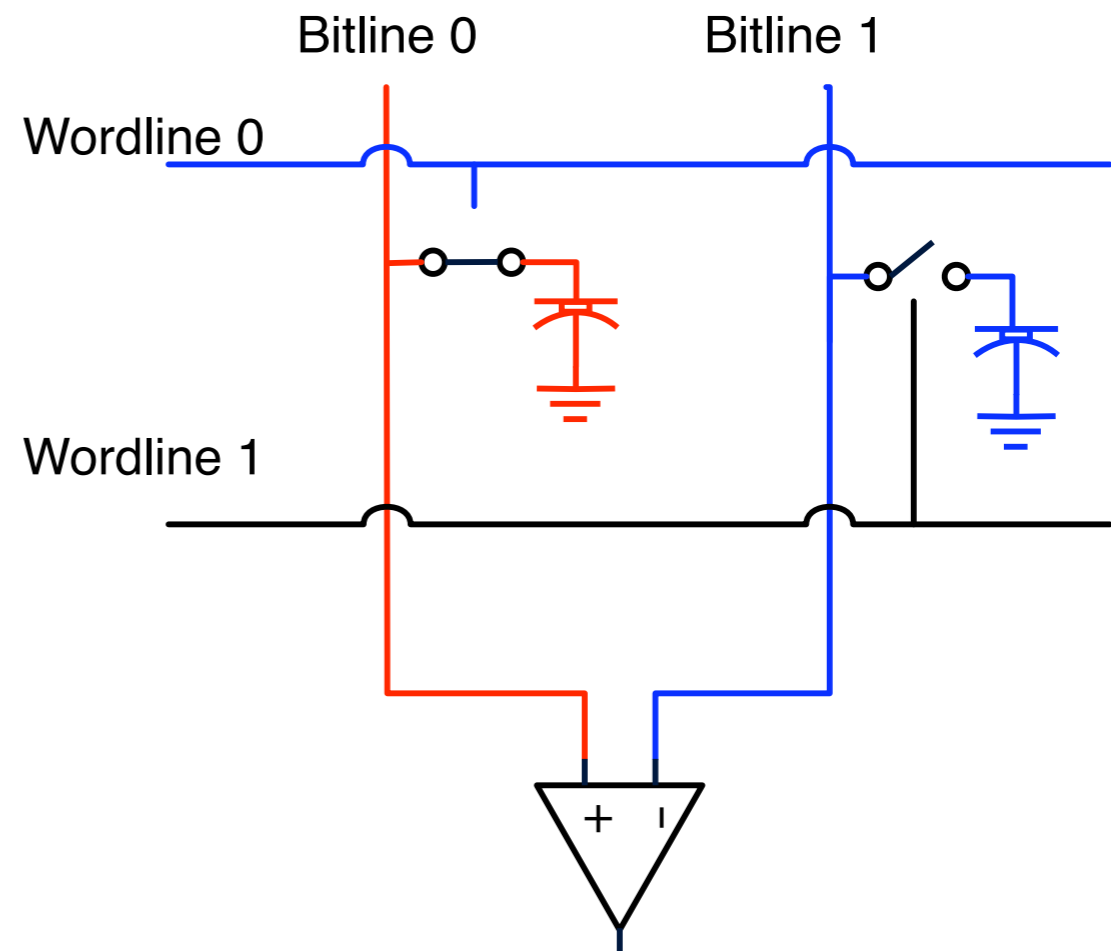
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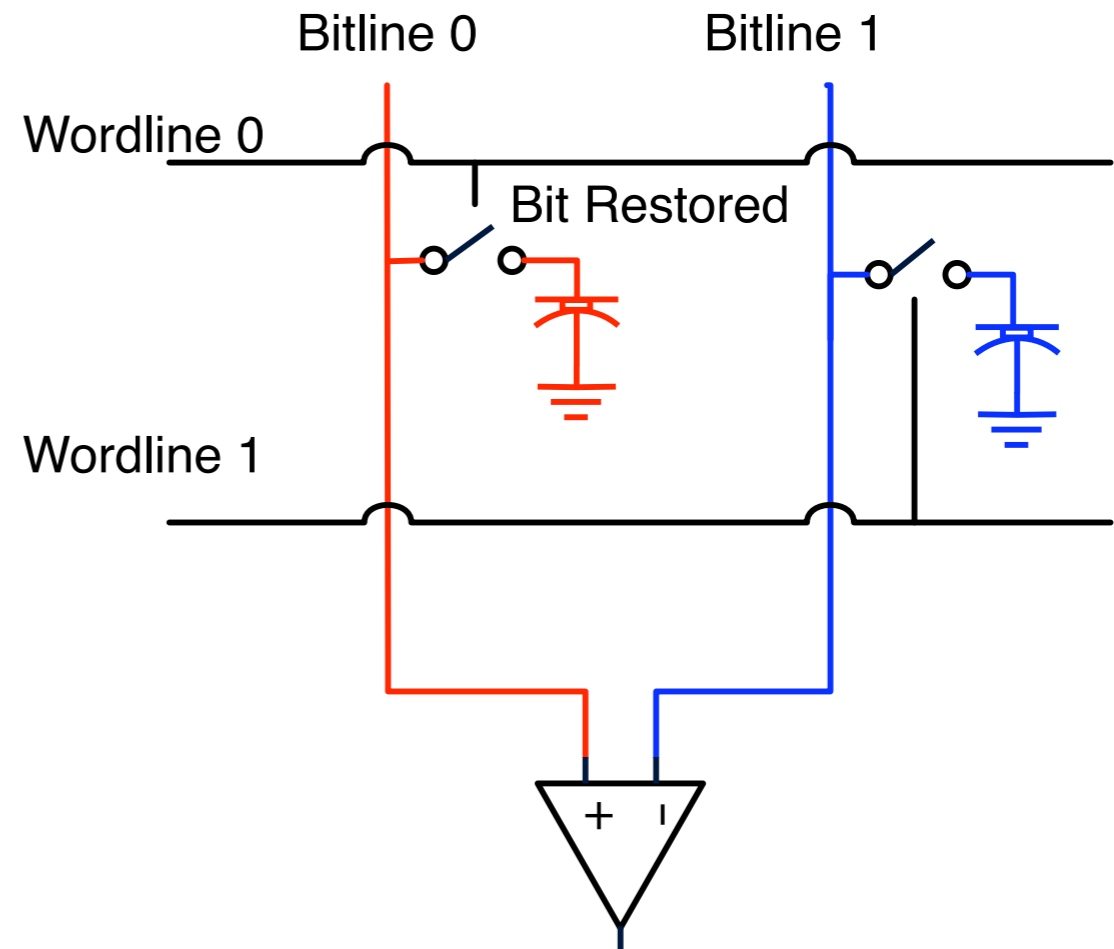
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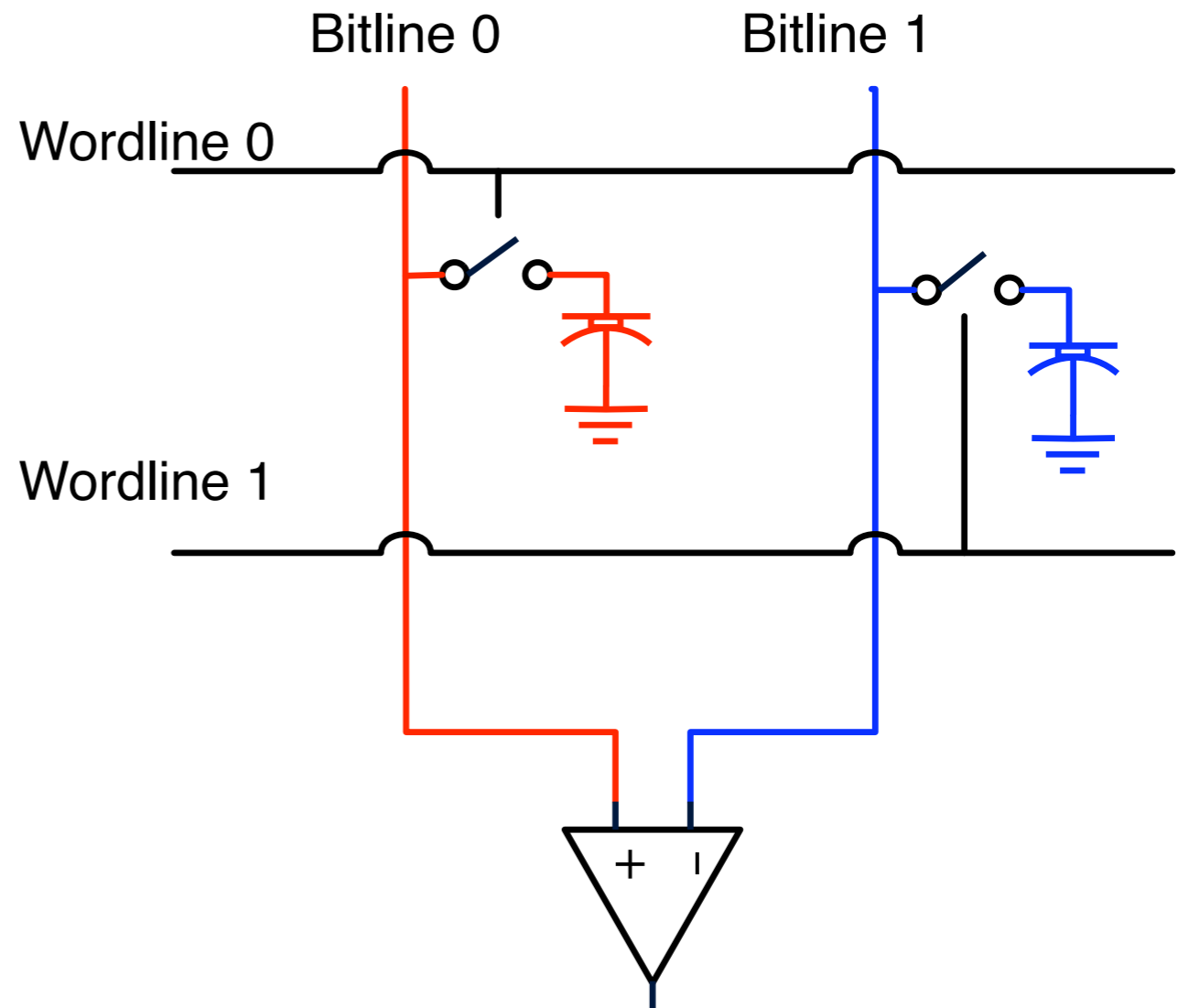
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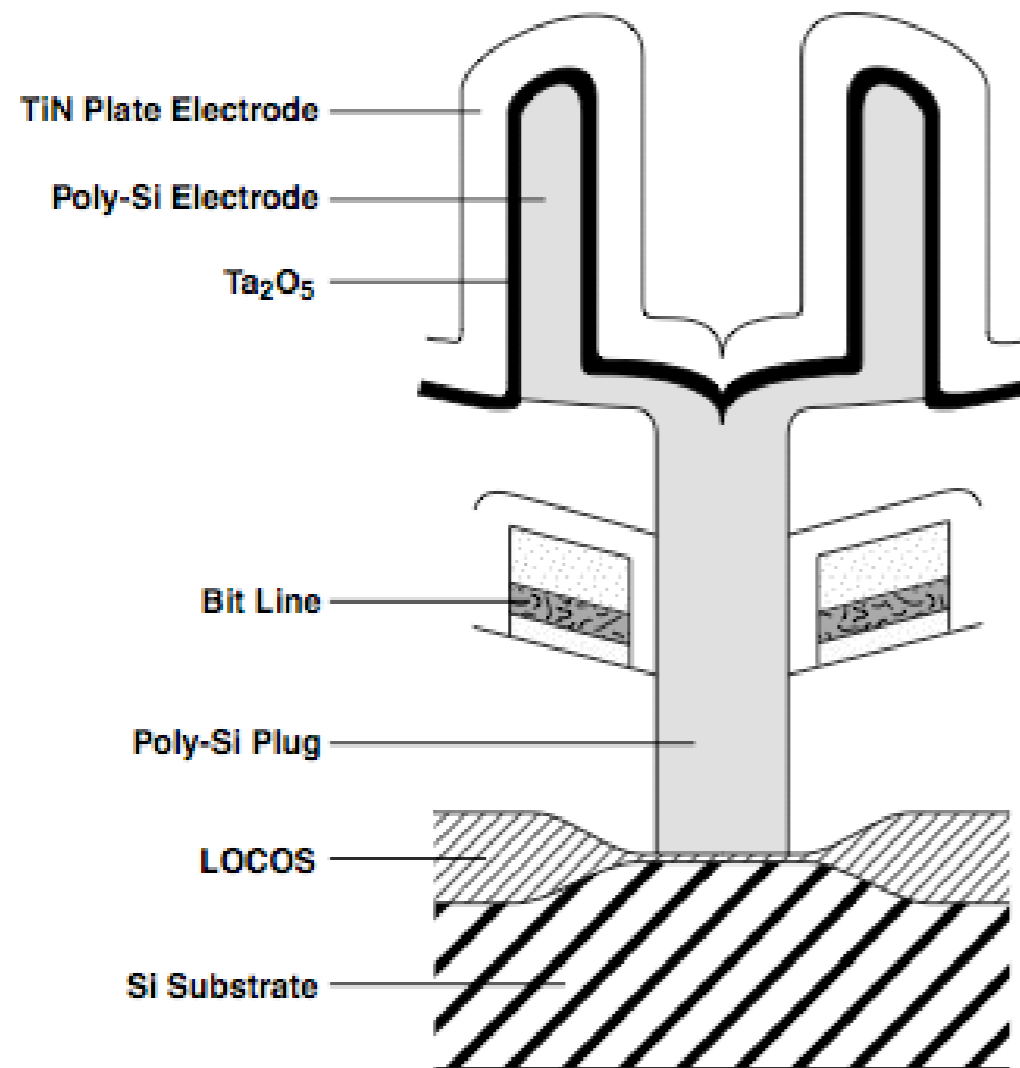


# DRAM: Write and Refresh

- **Writing**
  - Turn on the wordline
  - Override the sense amp.
- **Refresh**
  - Every few micro-seconds, read and re-write every bit.
  - Consumes power
  - Takes time

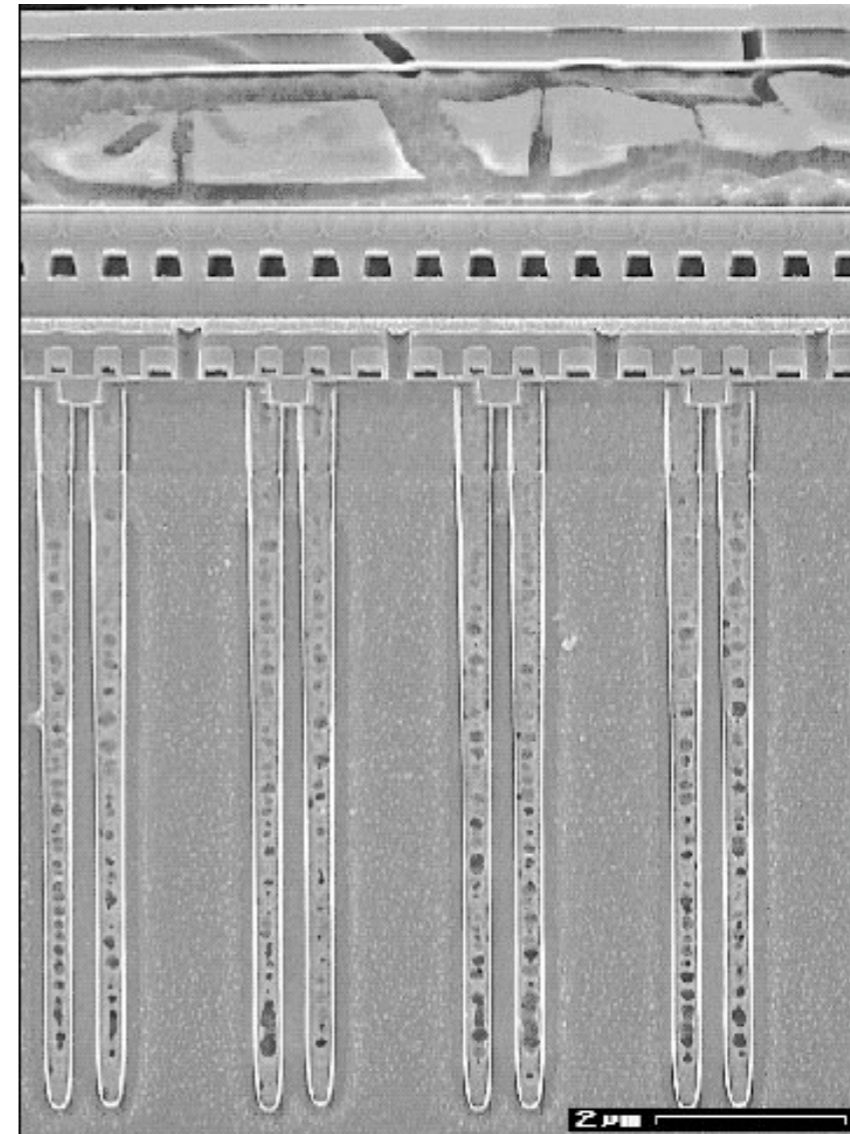


# DRAM Lithography



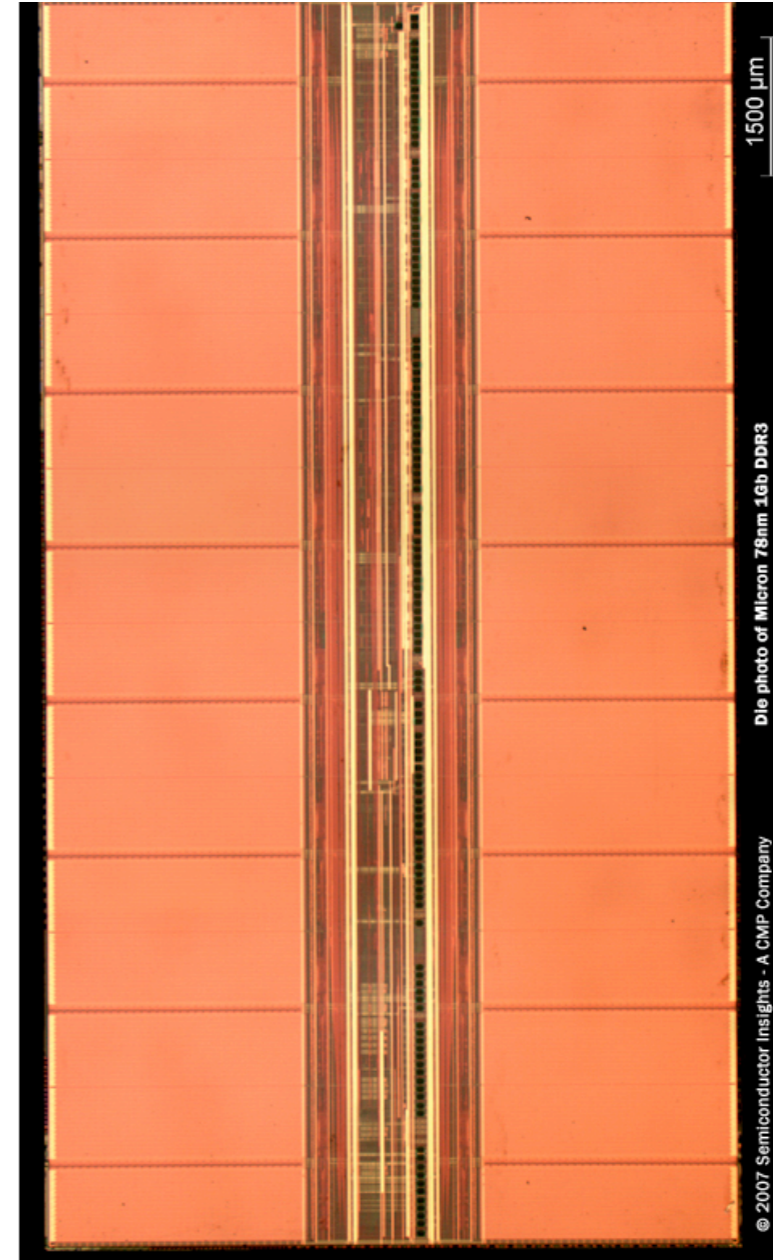
Source: HitachiVCE, "Memory 1997"

20766



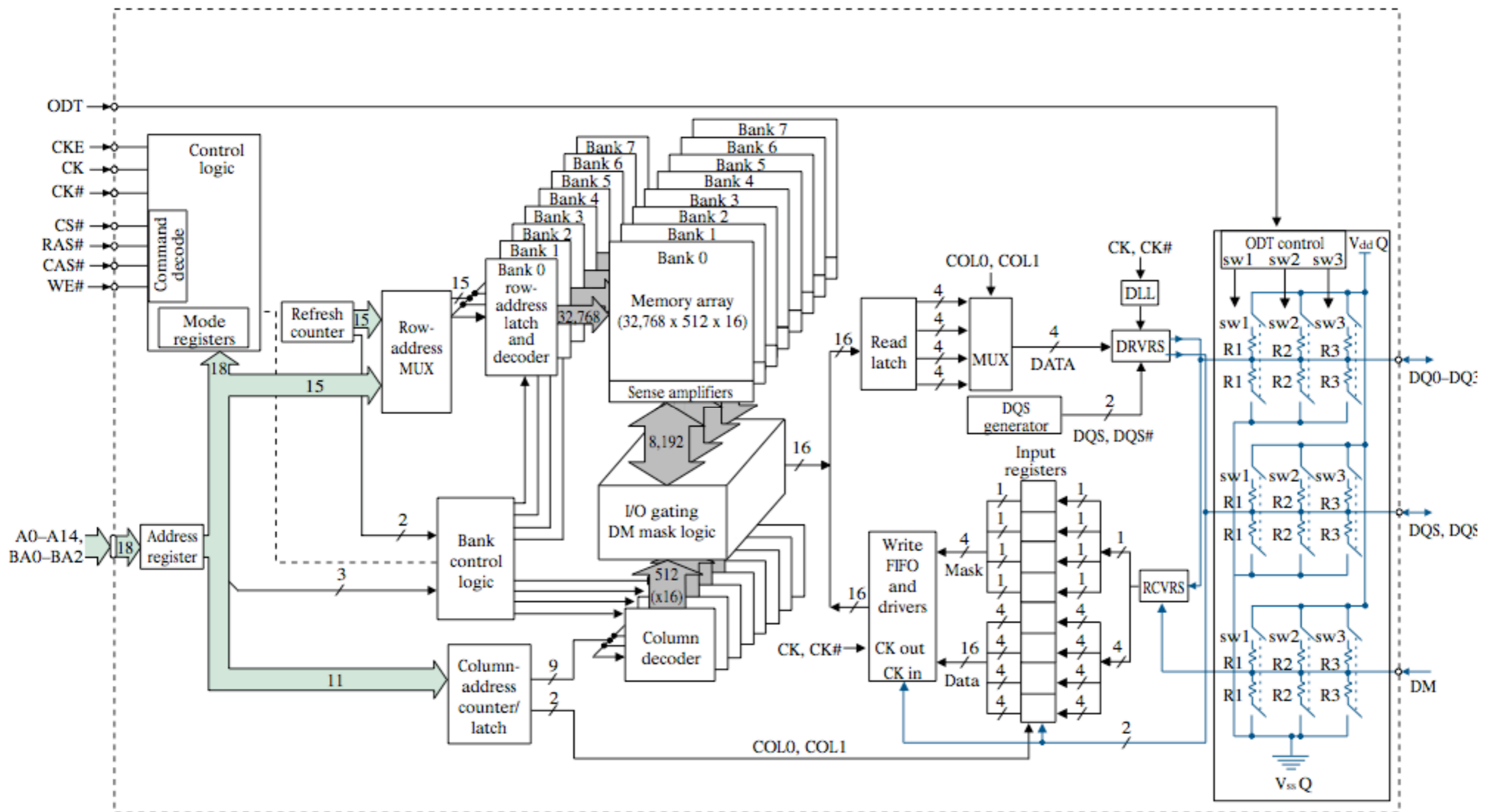
# DRAM Devices

- There are many banks per die (16 at left)
  - Multiple can be active at once to hide latencies
  - Parallelism!!!
- Example
  - open bank 1, row 4
  - open bank 2, row 7
  - open bank 3, row 10
  - read bank 1, column 8
  - read bank 2, column 32
  - ...

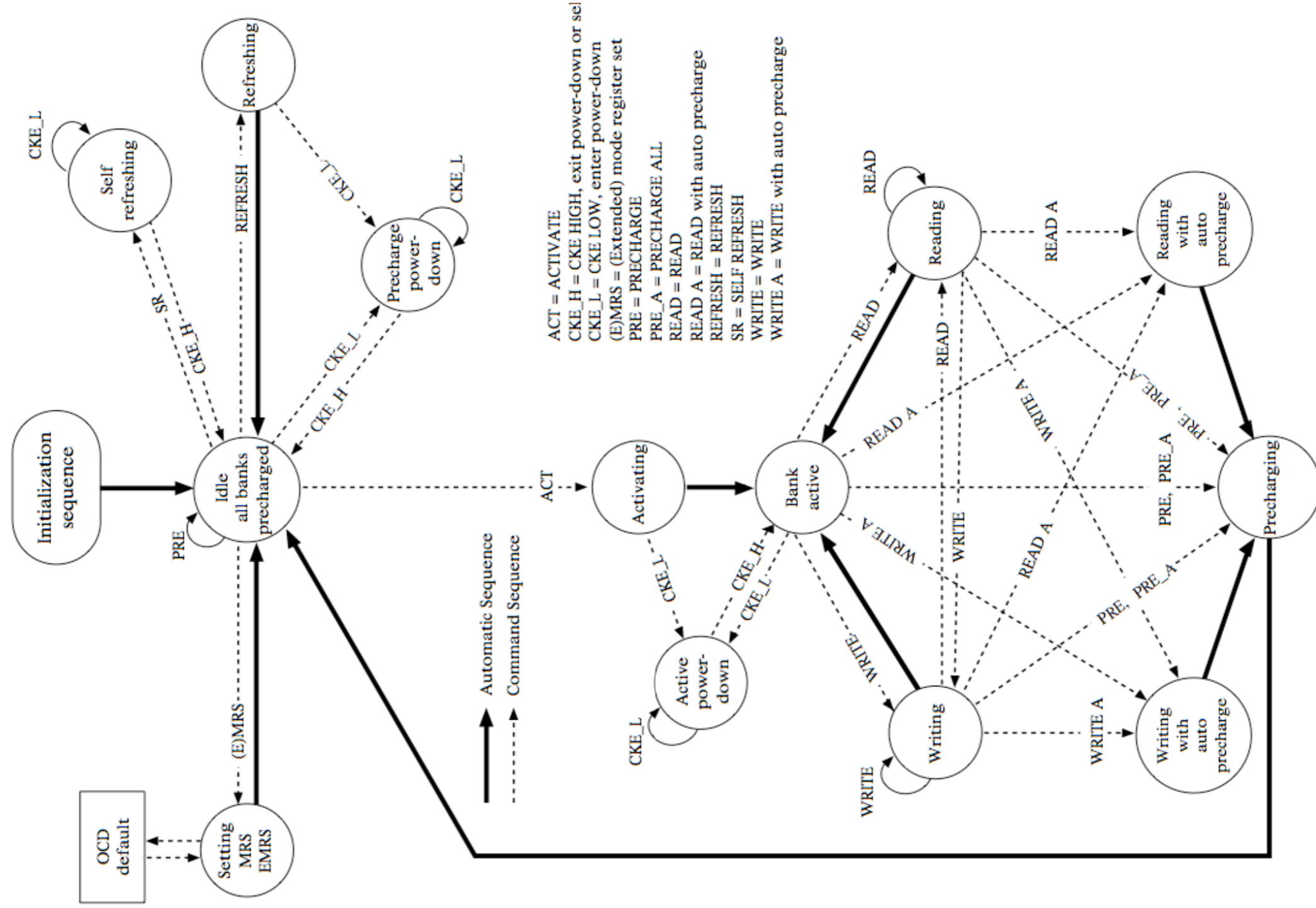


Micron 78nm 1Gb DDR3

# DRAM: Micron MT47H512M4



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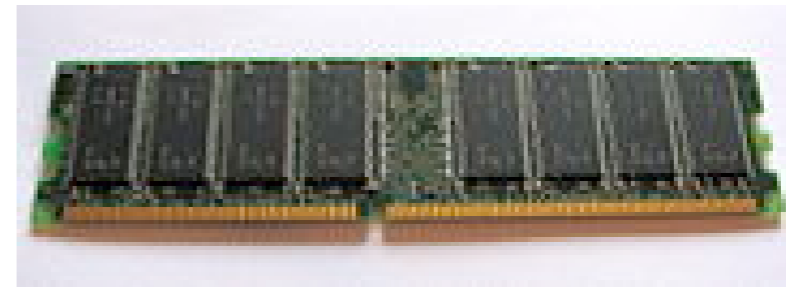


# DRAM Variants

- The basic DRAM technology has been wrapped in several different interfaces.
- SDRAM (synchronous)
- DDR SDRAM (double data-rate)
  - Data clocked on rising *and* falling edge of the clock.
- **DDR2**
  - Example on previous slides
- DDR3
- **RDRAM**
  - Rambus RAM
- GDDR2-5 -- For graphics cards.
- **FB-DIMMS**

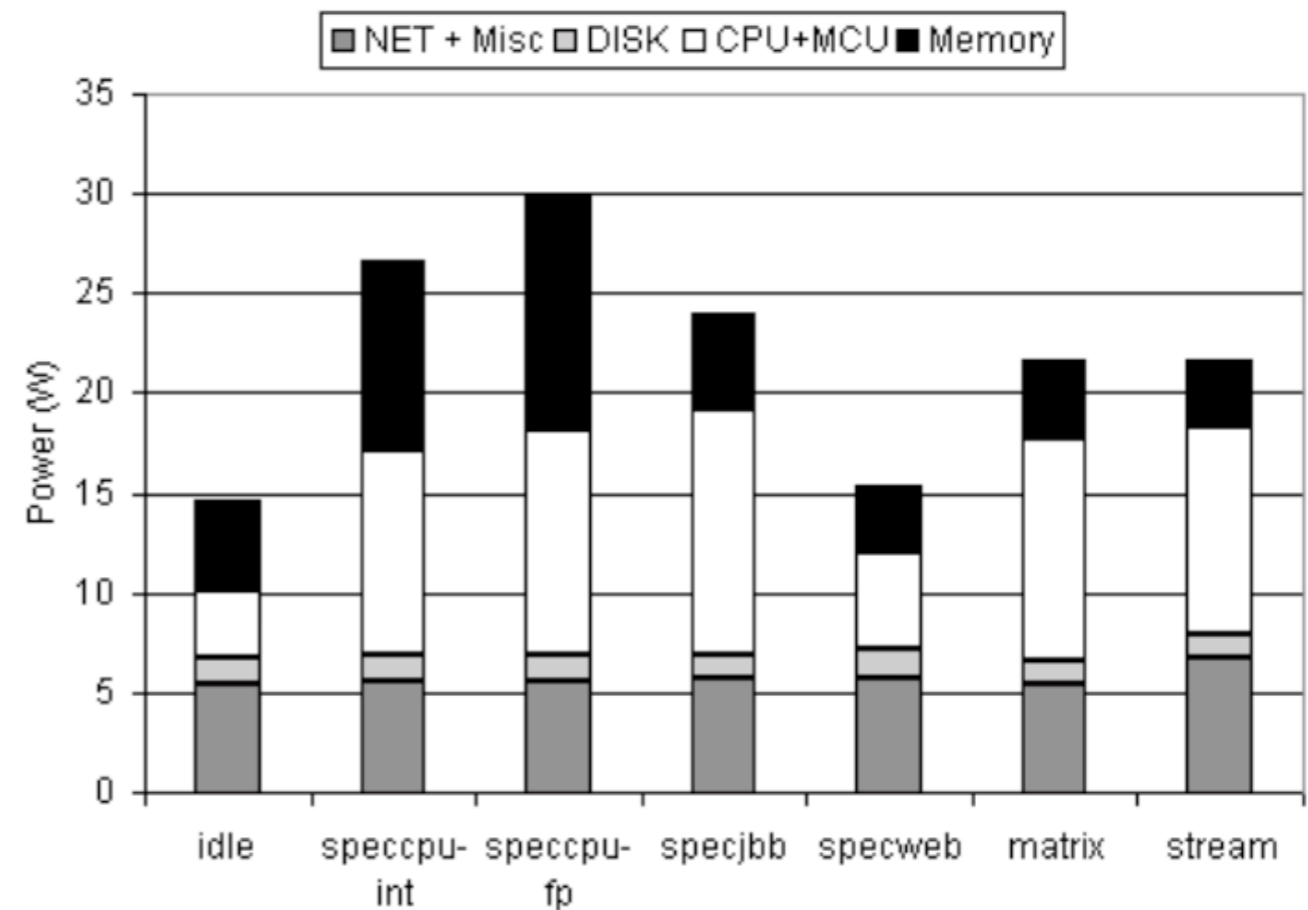
# DDR2 SDRAM

- Fewer, larger banks.
- Pin count per package (DIMM): 14 address, 16 data
- DIMM data path is 64bits
- Data rate: up to 800Mhz DDR (1600Mhz effective)
- Bandwidth per DIMM GTNE: 12.8GB/s
  - *guaranteed not to exceed*
- Multiple DIMMs can attach to a bus
  - Reduces bandwidth/GB (a good idea?)



# Power

- DRAM is a major power sink.
- Idle power: 2-4W/  
DIMM
- Active power: 5-8W/  
DIMM



Economou, et. al 2006

# DRAM Scaling

- Long term need for performance has driven DRAM hard
  - complex interface.
  - High performance
  - High power.
- DRAM used to be the main driver for process scaling, now it's flash.
- Scaling is expected to match CMOS tech scaling
- $F^2$  cell size will probably not decrease