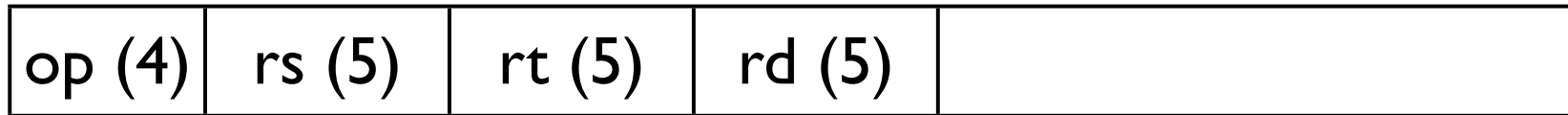
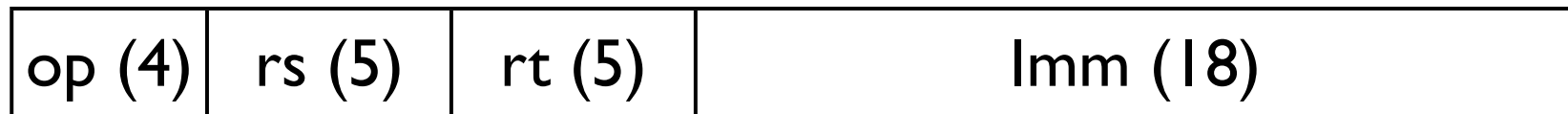


## R-Type (so far)



## I-Type (so far)



## RTL (register transfer language):

```
Inst = mem[PC]
rs = Inst[26:22]
rt = Inst[21:17]
...
Imm = Inst[17:0]
SignExtendImm = SignExtend32(Imm)
```

```
add:  R[rd] = R[rs] + R[rt]
      PC = PC + 4
addi: R[rt] = R[rs] + SignExtendImm
      PC = PC + 4
addui: R[rd] = R[rs] + zeroExtendImm
      PC = PC + 4
sub:  R[rd] = R[rs] - R[rt]
      PC = PC + 4
subi: R[rd] = R[rs] - SignExtendImm
      PC = PC + 4
```