Open Source Hardware

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What is Open Source Hardware?

- “Open Hardware is a thing - a physical artifact, either electrical or mechanical - whose design information is available to, and usable by, the public in a way that allows anyone to make, modify, distribute, and use that thing.”
  - TAPR Open Hardware License
The "Source" may include:

- Mechanical Diagrams
- Schematics and Circuit Diagrams
- Bill of Materials
- Layout Diagrams
- HDL or Firmware
- Interface Software/API
Open Source EDA

- Some definitions of “open source” require open source development tools
- Open source EDA tools are not as mature as GNU toolchain
- Proprietary tools are often required
Why O.S.H. is becoming popular

- Better and cheaper FPGAs and CPLDs
- Market shifts toward SoC design
- Success of Open Source Software movement
Arduino

- Prototyping platform for AVR Atmega microcontrollers
- Schematics, EAGLE files, and development tools are open source

- Other manufacturers and hobbyists have made variations of the Arduino
Open Graphics Project

- Goal is to produce a fully open graphics card with open specs and open source drivers

**OGD1 Open Graphics Development Board**

- 8x 256 MiB DDR RAM (4 on reverse side)
- 2x Dual-Link DVI Transmitters
- 100-pin Expansion Connector

Xilinx® Spartan™-3 XC3S4000 FPGA

Lattice™ XP10 FPGA
**Oscar**

- Goal is to “develop a car according to Open Source principles.”
- Shows how far-reaching the open source movement has become
Open HDL Cores

- The real potential of open source hardware lies in open HDL modules
  - Need for easy SoC integration
  - Modification and redistribution is easy
- Repositories for Open HDL Cores have emerged, most notably: OpenCores.org
OpenCores.org

- Over 200,000 registered users, 397 projects
- Compare to Sourceforge: over 1.9 million registered users, over 138,000 projects
- Core types include:
  - Processor cores
  - DSP cores
  - Memory cores
  - Communication controllers such as Ethernet, I2C, SPI, CAN, USB, PCI
  - Video controllers
WISHBONE

- Interconnect standard used by many cores on OpenCores
- Developed by Silicore Corporation
- Transferred stewardship to OpenCores in 2002
- Goal is simplicity, flexibility, and OPENNESS
- Master/Slave
- Multiple topologies are supported:
  - Point-to-point
  - Data flow
  - Shared bus
  - Crossbar
OpenRISC

- 32 or 64-bit address space
- Basic Instruction Set can be extended:
  - Vector/DSP extension
  - Floating-point extension
  - User-provided instructions
- Number of registers and cache sizes are configurable
- Ported to OpenRISC:
  - GCC, GNU Binutils, uClibc, BusyBox, Linux, uCLinux, RTEMS
JOP: Java Optimized Processor

- Started as a PhD thesis, now has wide community support
- Hardware RISC implementation of JVM
- Provides predictable timing for hard real-time systems
A few other projects

- ZPU – the world's smallest 32 bit CPU with GCC toolchain
- Zet – the x86 open implementation
- 8051 core
- AVR core
- JPEG Hardware Compressor
- PAL/NTSC encoder
- AC 97 Controller IP Core
- PS2 Interface
The future of O.S.H.?

- Probably will not be as strong as open source software movement
- May become a powerful force in SoC and embedded systems design