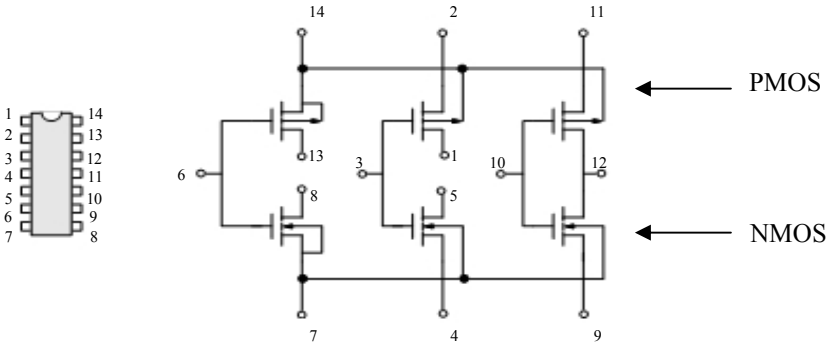
ECE 53A: Fundamentals of Electrical Engineering I

Laboratory Assignment 3: MOS Logic Gates
Fall 2007

Note: In this Lab we use CD4007 chip that consists of 3 pairs of complementary n-channel and p-channel MOSFETs. One pair is internally wired as a CMOS inverter. The pin arrangement for the chip is shown below. You need to power the chip by attaching a 5 V supply to pin 14 (V_{DD} = 5 V) and grounding pin 7. You can assume V_T = 1.4 V for your calculations.

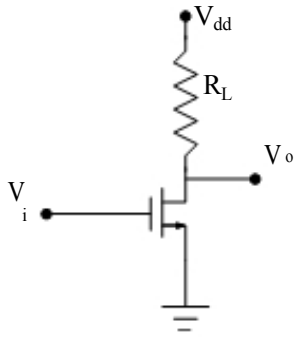


Part A - n-channel MOS inverter:

Lab Exercise:
For this experiment use the n-channel MOS inverter that is attached to pins 6, 7, and 8. Assemble the circuit below on the protoboard, using R_L = 2.2 kΩ. Set up the function generator to produce a triangular wave with peak-to-peak amplitude of 5 V and a DC offset of 2.5 V. In this case, the wave is a triangle between 0 and 5 V. Apply this signal to the input of the gate. Attach scope channel A to the input and scope channel B to the output. Set the scope display to XY mode (persistence of 1 s). You should see the transfer characteristics of the inverter circuit on the scope display.

a) Make a hard copy and on the hard copy, draw V_i and V_o axes and label and mark the voltage scales. Identify regions in which MOS is in cut-off, linear, and saturate regions.

b) Read values of V_o for V_i = 2.5 and 5 V from your graph. In each case, solve the MOS circuit and find the value of the parameter K (in MOS I_{DS} , V_{DS} equations).



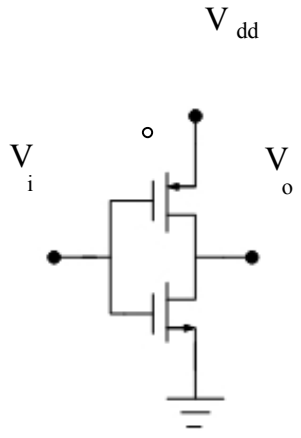
Part b - CMOS inverter:

Lab Exercise:
For this experiment use the CMOS inverter that is attached to pins 9 through 12.

a) Assemble the circuit below on the protoboard. As in part A, set up the function generator to produce a triangular wave with peak-to-peak amplitude of 5 V and a DC offset of 2.5 V. Apply this signal to the input of the gate. Attach scope channel A to the input and scope channel B to the output. Set the scope display to XY mode (persistence of 1s). You should see the transfer characteristics of the inverter circuit on the scope display. Make a hard copy and on the hard copy, draw V_i and V_o axes and label and mark the voltage scales.

b) A major advantage of CMOS inverter is that it draws zero current when it is in high or low state. However, the drain current is not zero when CMOS is transitioning between states. To see this, attach a 100 Ω resistor between pin 7 and ground. The voltage across this resistor will be proportional to drain current. Apply the triangular wave above to the input of the gate. Attach scope channel A to the input and scope channel B to the 100 Ω resistor. Set the scope display to XY mode (persistence of 1 s). You should see a plot of I_D vs V_i . Make a hard copy and on the hard copy, draw V_i and I_D axis and label and mark the voltage and current scales.

c) Comment on the relative advantages and disadvantages of the CMOS inverter over those of the n-channel inverter of part A.



Part c - NAND and NOR connections:

Lab Exercise:
For this experiment use the CMOS inverter that is attached to pins 9 through 12 and MOS transistors with the gate connected to pin 6.

1) Draw the circuit diagram of a two-input NAND gate. Identify chip pins on the circuit diagram and explain which pins should be connected together. Wire your chip to make a two-input NAND gate. Test your NAND gate with attaching a 1 kHz square wave (0-5 V) to pin 6 and a DC voltage of either zero or 5 V to pin 10. In each case, make a hard copy. Describe the output waveform in each case and explain how it corresponds to the NAND of the two inputs, using a truth table format.

1) Draw the circuit diagram of a two-input NOR gate. Identify chip pins on the circuit diagram and explain which pins should be connected together. Wire your chip to make a two-input NOR gate. Test your NOR gate with attaching a 1 kHz square wave (0-5 V) to pin 6 and a DC voltage of either zero or 5 V to pin 10. In each case, make a hard copy. Describe the output waveform in each case and explain how it corresponds to the NOR of the two inputs, using a truth table format.