Historical Context:
Simplifying Control Design Through Microprogramming

The Problem with FSMs as control sequencers

• They get unmanageable quickly as they grow.
  – hard to specify
  – hard to manipulate
  – error prone
  – hard to visualize

Implementing a control FSM

<table>
<thead>
<tr>
<th>Opcode</th>
<th>State Reg</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inputs</td>
<td>Outputs</td>
</tr>
<tr>
<td></td>
<td>Control Logic</td>
</tr>
</tbody>
</table>

Implementing a control FSM with ROM

Each line in the ROM contains control signal outputs (an operation), and next-state outputs (branch destination)
Implementing a control FSM with a microprogram

Each line in the ROM is now a microprogram instruction, corresponding to a FSM state, with an operation (control signals) and branch destination (next state info).

Microprogram Implementation

- Being able to specify sequences of signals doesn’t necessarily make it “easy”.
- Groups of signals are combined and given symbolic names. E.g.,
  - MemRead, ALUSrcA = 0, IorD = 0, ALUSrcB = 01… = “fetch”
  - RegDst=1, MemtoReg=0, regwrite=1 => “rd = ALUout”
  - RegDst=0, MemtoReg=1, regwrite=1 => “rt = MDR”
- So a microprogram might be:
  
  start: fetch
decode; goto “opcode”

  ... 

  add: src1=A; src2=B; add
rd=ALUout; goto start
A Microprogram

<table>
<thead>
<tr>
<th>Label</th>
<th>ALU control</th>
<th>SRC1</th>
<th>SRC2</th>
<th>Register control</th>
<th>Memory</th>
<th>PCWrite control</th>
<th>Sequencing</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fetch</td>
<td>Add</td>
<td>PC</td>
<td>4</td>
<td>Read PC</td>
<td>ALU</td>
<td>Seq</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Add</td>
<td>PC</td>
<td>Exshft</td>
<td>Read</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Mem1:</td>
<td>Add</td>
<td>A</td>
<td>Extend</td>
<td></td>
<td>Dispatch 1</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>LW2:</td>
<td></td>
<td>Read ALU</td>
<td></td>
<td>Seq</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>SW2:</td>
<td></td>
<td>Write MDR</td>
<td></td>
<td>Fetch</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Rformat1:</td>
<td>Func code</td>
<td>A</td>
<td>Write ALU</td>
<td>Fetch</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>BEQ1:</td>
<td>Subt</td>
<td>A</td>
<td>Write ALU</td>
<td>ALUOut-cond</td>
<td>Seq</td>
<td>Fetch</td>
</tr>
<tr>
<td></td>
<td>JUMP1:</td>
<td></td>
<td>A</td>
<td>ALUOut-cond</td>
<td>Jump address</td>
<td>Seq</td>
<td>Fetch</td>
</tr>
</tbody>
</table>

Microprogramming

- If a microprogram is fundamentally the same as the FSM, what’s the big deal?
  - Easier to specify (program), visualize, and manipulate.
  - allows us to think about the control symbolically
- Each microinstruction typically specifies (1) control information and (2) sequencing information (which microinstruction to execute next).
- There would typically be a one-one correspondence between FSM states and microprogram instructions.
- Microprogramming allowed architectures to change/adapt/be fixed easily. It is also to blame for the extreme CISC architectures. Why?

Exceptions

- There are two sources of non-sequential control flow in a processor
  - explicit branch and jump instructions
  - exceptions
- Branches are synchronous and deterministic
- Exceptions are typically asynchronous and non-deterministic
- Guess which is more difficult to handle?

(control flow refers to the movement of the program counter through memory)
Exceptions and Interrupts

the terminology is not consistent, but we’ll refer to
• exceptions as any unexpected change in control flow
• interrupts as any externally-caused exception

So then, what is:
  – arithmetic overflow
  – divide by zero
  – I/O device signals completion to CPU
  – user program invokes the OS
  – memory parity error
  – illegal instruction
  – timer signal

For now...

• The machine we’ve been designing in class can generate two types of exceptions.
  –
  –
  –

• On an exception, we need to
  – save the (invisible to user code)
  – record the nature of the exception/interrupt
  – transfer control to OS

Handling exceptions

• PC saved in EPC (exception program counter), which the OS may read and store in kernel memory
• A status register, and a single exception handler may be used to record the exception and transfer control, or
• A vectored interrupt transfers control to a different location for each possible type of interrupt/exception

Supporting exceptions

• For our MIPS-subset architecture, we will add two registers:
  – EPC: a 32-bit register to hold the user’s PC
  – Cause: A register to record the cause of the exception
    • we’ll assume undefined inst = 0, overflow = 1
• We will also add three control signals:
  – EPCWrite (will need to be able to subtract 4 from PC)
  – CauseWrite
  – IntCause
• We will extend PCSource multiplexor to be able to latch the interrupt handler address into the PC.
Supporting exceptions in our DataPath

Shift left 2
Memory
MemData
Write data
Mux

Instruction
[15–11]
Mux
0
1

Instruction
[15–0]
Sign extend
32
16
Instruction
[25–21]
Instruction
[20–16]
Instruction
[15–0]
Instruction
register

ALU
control

ALU
result

ALU
Zero

Memory
data
register

A
B
IorD
MemRead
MemWrite
MemtoReg
PCWriteCond
PCWrite
IRWrite

Control
Outputs

Op
[5–0]

Instruction
[31-26]
Instruction
[25–0]
Instruction
[26]
Instruction
[28]
Jump address [31-0]
Shift left 2
PC [31-28]

Instruction
[19–15]
Instruction
[14–10]
Instruction
[9–5]
Instruction
[4–0]

ALUSrcA = 0
IRWrite
ALUSrcB = 01
ALUOp = 00
MemRead

PCSource = 00
MemWrite

RegDst = 1
MemtoReg = 0
RegWrite

ALUSrcA = 1
ALUSrcB = 00
ALUOp = 10

RegDst = 1
MemtoReg = 0

overflow

To state 11

To state 0

Supporting exceptions in our FSM.

Instruction Fetch, state 0
Instruction Decode/ Register Fetch, state 1

Supporting exceptions in our FSM.
Key Points

- Microprogramming can simplify (conceptually) CPU control generation.
- A microprogram is a small sequencer/processor inside the CPU that executes the individual instructions of the “real” program.
- Exception-handling is difficult in the CPU, because the interactions between the executing instructions and the interrupt are complex and sometimes unpredictable.