For Lab 1

The following questions are specific to Xilinx 6.3.i design environment on CSE B240/B250 computers

1. During the Implementation Design step, the following error message pops up,
   The instruction at “0x0065e49” referenced memory at “0x517c812f”. The memory can not be read.
   and the Implementation Design step can not proceed. What should I do?

   A: Unfortunately, we don’t have a solution to this problem yet. ACS stuff are still working on it. The problem seems to be random on different machines, so the only thing you can do is switching to another machine. We have compiled a list of machines that do not encounter this problem. See the following map.

<table>
<thead>
<tr>
<th>Door</th>
<th>B250</th>
</tr>
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<tbody>
<tr>
<td>1</td>
<td>2</td>
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<td>12</td>
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<td>13</td>
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<td>35</td>
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<td>37</td>
<td>38</td>
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</tbody>
</table>

Legend
- Untested
- Good
- Bad
2. I get the following warning message after the Implementation Design step is done:

```
WARNING:SpeedCalc:42 - Cannot find referenced model "bel_d_min_period". This generally indicates that there is an inconsistency between versions of the speed and device data files. Please check to ensure that the XILINX environment variable is set correctly, if the MYXILINX variable is set, make sure that it is pointing to patch files that are compatible with the version of software that the XILINX variable points to.
```

What does it mean?

A: The warning message is due to a bug of the software associated with the device we chose (i.e. Spartan2 xc2s30-5tq144). Nevertheless, it is irrelevant for our project so you can just ignore it.

3. I saved my project in a local directory of the computer, but the next day when I came to the same computer and login, my project files are gone! How could it be?

A: Yes. Files stored in local directories such as \workarea will automatically get erased when you logout. Instead, save your project in your personal ACS network directory.

The following questions are general to Lab1.

4. How many test vectors are required for the 4-bit adder?

A: The 4-bit adder has 9 inputs and a total of 512 test vectors is needed to cover all the possible input combinations. Although there are ways to automate test vector generation in the testbench waveform, that’s still too cumbersome. Therefore, for the 4-bit adder we only require 10~20 test vectors in the testbench waveform.

5. I have the worst case delay from the timing report, but how can I show it on the ModelSim post-place & route simulation waveform?

A: Let’s take the 4-bit adder as an example. Suppose from the timing report we know the worst case delay is 8.570ns from A1 to Co. To see this delay on the post-
place and route simulation waveform you need to create a test case in which Co changes *solely* because of the change of A1. For example, keep a4a3a2=111, b4b3b2b1=0001 and Ci=0, let a1 change from 0 to 1. In this case Co will also experience a transition from 0 to 1. You can see the worst case delay of 8.57ns from this test case.