

H&P problems 5.3 (or 5.2a-e), 5.4a-e, 5.8, P1, P2, P3, W3.

P1. You know a particular cache required 1059 bits per set to implement the cache, including tag, data, valid, and LRU bits. What do you know about the organization of the cache (e.g., size, associativity, line size)? Assume the processor has 32-bit virtual and physical addresses.

P2. I am designing a pseudo-associative cache, and I want it to have the following properties:

- maximize the number of regular (fast) hits
- the total hit rate (regular + pseudo hits) is exactly the same as for a 2-way set-associative cache.

What must my lru tracking, line replacement, and line swap strategy be? Be specific.

P3. Calculate the cache hit rate for the following trace of memory accesses and cache configurations. The caches are all 128 bytes total size. Addresses are byte addresses.

Address	a)16-byte block size, 4-way set associative	b)32-byte block size, direct mapped
4 (00000100)	<i>miss</i>	
8 (00001000)		
16 (00010000)		
20 (00010100)		
128 (10000000)		
160 (10100000)		
128 (10000000)		
140 (10001100)		
144 (10010000)		
148 (10010100)		
4 (00000100)		
8 (00001000)		
16 (00010000)		
Overall Miss rate?		

(c) Give the values of all (known) tag fields in the cache at the end of the trace for the cache in (b), the last column. Assume addresses are 8 bits wide.

W3. For the following processors:

Alpha 21264, 21364, Intel Itanium, Pentium 4, AMD Athlon  
Tell me the size and associativity of all on-chip caches.