CSE140 Fall 2002, Exercise

I. A state machine is described by the following state equations.

\[ Q_0(t + 1) = Q_1'(t)x'(t) + Q_1(t)x(t), \]
\[ Q_1(t + 1) = Q_0(t) + Q_1(t)Q_0'(t)x(t). \]

I(1). Write the state table.
I(2). Design the system with 2 T flip-flops and a minimal number of 4-input multiplexers.

II. Given a modulo-16 counter, draw the logic diagram to show the following designs.

II(1). Design a 2-to-15 counter with a modulo-16 counter and a minimal NOR network (no other gates).
II(2). Design a counter with output sequence 0, 1, 2, 10, 11, 3, 14, 15 with a modulo-16 counter and a minimal combinational network. Assume that the machine is reset to 0 initially. Draw the schematic diagram.

III. Adders: Draw the logic diagram to show the following designs.

III.(1). Design a full adder with a minimal number of 2:1 multiplexers (no other gates). Draw the schematic diagram.
III.(2). A sequential adder inputs \( ai, bi \), the \( i \)'th bit of two binary numbers in each clock cycle for \( i = 0 \) to \( n - 1 \) and outputs the sum. Implement the adder with a SR flip-flop and a minimal two level NOR network (no other gates). Draw the schematic diagram.

IV. System Designs:

Implement the following algorithm:

Alg: { Input \( X<0:7> \), \( Y<0:7> \) type bit-vector,
  start type boolean;
  Local-object \( A<0:7> \), \( B<0:7> \) type bit-vector;
  Output \( W<0:7> \), \( Z<0:7> \) type bit-vector,
  done type boolean; }

S1: If start' goto S1;
S2: done<- 0 || A<- X || B<- Y || W<- 0;
S3: A<- Add(A,B) || W<- Inc(W);
S4: If A'<7> goto S3;
S5: Z<- A || done<- 1 || goto S1
end Alg

IV(1). Design a data subsystem that is adequate to execute the algorithm. Draw the schematic diagram to show the design.
IV(2). Design the control subsystem (i) draw the state diagram; (ii) draw the logic diagram that implements the control subsystem with a one hot encoding design.