Generation of Design Guarantees for Interconnect Matching

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ABSTRACT

Manufacturable design requires matching of interconnects which have equal nominal dimensions. New design rules are projected to bring guarantee rules for interconnect matching. In this paper, we present a methodology to generate additional guarantees given the limited set of guarantees in the design manual. In order to achieve this, we propose a multi-function optimization method to extract parameters of a preliminary dimension- and distance-based process correlation model for interconnects. We propose an interconnect matching extraction method and suitable patterns useful for mismatch extraction. We have extracted matching guarantees while also considering the special case of edge matching using Monte Carlo analysis and field solvers. We have substantiated the experimentation with evaluations on a preliminary regression model and metric for mismatch.

Categories and Subject Descriptors

J.6 [**Computer-Aided Engineering**]: [CAM, CAD]

General Terms

design, algorithms

Keywords

interconnect matching, design guarantee generation, DFM

1. INTRODUCTION

Aggressive reduction of feature sizes, voltage levels and path delays make design constraints harder to achieve in every new technology. New methods must be identified so that unachievable or hard to achieve constraints can be relaxed to manageable levels. Efforts in [1] and [2] target crosstalk noise and RLC delay pessimism reduction respectively. One such method is necessary for interconnect matching. Interconnect delay is projected to dominate in newer technolo-

gies. For matched interconnects, design guarantees can be generated so that delay constraints related to a strict matching condition can be avoided. This may help in saving area, reducing design pessimism, decreasing design time or optimizing design.

Process variations over interconnects are known to dominate for 65nm technologies and beyond. Certain interconnects are designed "nominally equal", meaning that the designed values for the length, width and height are the same. The environment effects on the design can be considered to ensure nominal equality of matched interconnects by: **(i)** designing a symmetric pattern around the matched interconnects, or **(ii)** setting the density of metals in the environment of the two interconnects as the same, or **(iii)** running chemical-metal polishing simulations over the neighborhood of the matched interconnects and ensuring that the output yields nominally equal dimensions for the matched interconnects. Yet, process variations end up causing a mismatch of dimensions in the manufactured chip even after such considerations.

Upcoming back-end design rules are projected to include a guarantee on the amount of mismatch for certain dimensions. These guarantees state that, as long as the interconnects have a cross-section area larger than a value given in the manual and the spacing between matched interconnects are smaller than a given value, a percentage mismatch in the capacitance of the matched interconnects is guaranteed. These guarantees can then be used within the CAD tools in the design cycle either for **(i)** performance estimation given the interconnect constraints or **(ii)** interconnect optimization[1] given performance constraints. Yet, since these guarantees are limited in number and hence yield large step-wise discrete changes from one rule to another, they will be of limited help to CAD optimizations. Generation of a continuum of such rules can yield a continuous transition from one area-spacing combination to another, thereby enabling aggressive optimization.

Given a set of limited matching guarantees, we seek a method to generate additional guarantees for dimensions not given in the manual. Such a method can be incorporated into the design tools or the DRC check tool. However, this process is not a straightforward extrapolation. One reason is that the number of design guarantees is so few that it is not possible to directly extrapolate the results. Secondly, the given guarantees do not lend any way to account for

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[1]Global clock tree optimization is one important application field due to its criticality.

extreme cases, e.g., the matching of two lines, one of which is at the edge of an array. Third, an extraction must first be applied to acquire the process variations that have led to the guarantees given in the manual. This requires an analytic model for process variations that can be optimized to the simulation data given in the design manual. A final issue is that we need to modify the standard capacitance extraction procedure to be able to account for mismatch.

2. PREVIOUS WORK

Process variations on matched structures result in mismatch. For interconnects, this mismatch can show its effects on electrical parameters such as resistance, capacitance or delay, although the source of a mismatch directly affects physical parameters like the dimensions of the interconnects. Mismatch has traditionally been a major problem for transistors. The most well known mismatch model in use today is Pelgrom's model [3], which states that increasing transistor channel area and decreasing the spacing between matched transistors decreases mismatch. In [4], mismatch is tied to physical reasons and models are formulated so that physical parameters instead of the resulting electrical parameters are used in the equations directly. This type of physics-based modeling is especially relevant to interconnects due to the presence of a directl relationship to physical parameters.

Interconnect performance in the presence of process variations has been analyzed in a number of papers. [5] has used Hilbert-space and orthogonal polynomial expansions for stochastic analysis of interconnects. [6] has introduced models for dielectric thickness variation induced by pattern dependency of the chemical mechanical polishing and metal width variation due to lithography bias. [7] has shown that there is a trade-off between C and RC delay variations due to the fringing capacitance and has proposed design guidelines to reduce variations. In [9], sensitivity analysis is used to relate delay to interconnect dimensions. As interconnect performance is projected to increasingly dominate the circuit delay, there is significant possibility for design constraint relaxation. Techniques have been presented to account for these variations. [10] has considered interconnect variation in cross-talk verification. [11] has studied technology scaling and process variation effects on clock skew. [12] has investigated interconnect variation effects for multi-level signaling. Capacitance extraction under process variations has been handled in [8]. However, there has not been any work on extraction for mismatch.

3. THE CORRELATION MODEL

We start by assuming an analytical interconnect matching correlation model similar to the Pelgrom mismatch model [3]:[2]

$$\rho = f(A, S) = (aA + b/S^2) \qquad (1)$$

Here, A is the cross-section area of the interconnect and S is the spacing between matched interconnects. The correlation function f is assumed to be in the form:

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[2]The proposed methodology in this paper can be applied regardless of the assumed correlation model.

$$f = \begin{array}{ccc} 1 & , & 1 < (a * A + b/s^2) \\ a * A + b/s^2 & , & 0 \le (a * A + b/s^2) \le 1 \\ 0 & , & (a * A + b/s^2) < 0 \end{array} \qquad (2)$$

Hence, correlation is assumed to be linearly proportional to the area and inversely proportional to the square of the spacing.

4. EXTRACTION OF PROCESS CORRELATION

4.1 Extraction for Mismatch

To understand the difference between standard extraction and extraction for mismatch, an overview of the procedure is helpful. Standard capacitance extraction for various spacing and dimension combinations is handled by using 2D or 3D field solvers over various interconnect structures such as parallel interconnects over a ground plane or a cross-over structure. To reduce the simulation time for arrays of multiple interconnects, typically three such parallel interconnects are used in a finite simulation mesh and the field solvers are used to extract the capacitances. The reason to use three lines is to introduce symmetry with respect to the line in the middle, so that the coupling capacitances to neighboring lines are accounted for. At the end of the simulation, only the capacitances that pertain to the middle interconnect are used, as the outside lines have less coupling. This simulation is repeated for a number of interconnect spacings and dimensions (width, length, height combinations) for each pattern, and then a regression analysis is used to fit an analytic model to the simulation data. The resulting fitted-analytical model can be used after appropriate model order reduction and signal integrity analysis flows in the timing analysis for any interconnect found in the design.

To simulate for mismatch, we need to add one more interconnect into the simulation box. We use the middle two lines to extract the matching data, as they are symmetric. The structure to be simulated for the parallel interconnects over a ground plane is shown in Figure 1. Yet, for mismatch, a statistical computation is furthermore necessary for each spacing and dimension combination as compared to standard extraction. The statistical step can be handled through Monte Carlo simulations.

4.2 Extraction of Correlation Model Parameters

To be able to generate design guarantees, information regarding the process must first be extracted from the limited number of guarantees provided. In order to do this, a correlation model is used to assign variations of the interconnect dimensions for each Monte-Carlo run.

$$C = M.M^T \qquad (3)$$

$$Z = MG \qquad (4)$$

Here, C is an nxn, positive-definite and symmetric correlation matrix where n is the number of interconnects in the simulation box. M can be found through Cholesky decomposition. M^T is the transpose of matrix M. Given $nx1$

vector G consisting of independent normal Gaussian random variables, vector Z gives a correlated set of random numbers. Elements of Z, Z_i, can then be used to calculate $W_i = Z_i * W_{std} + W_{mean}$, where W_i is the width of the ith interconnect, W_{std} is the standard deviation of the width dimension and W_{mean} is the mean of the width. Height dimension for the interconnects are assigned similarly using Z_i parameters, with the exception of using the standard deviation and mean of height random variable.

We need to first extract the two parameters, a and b, from the given design guarantees. Different A and S combinations are given in the design guarantees though. This means different correlation functions with respect to the parameters a and b need to be optimized at the same time. Standard multi-variate Newton-Raphson algorithm uses a single function to optimize. Hence, we propose a multi-function variant of multi-variate Newton-Raphson to extract correlation parameters a and b from the provided design guarantees:

Multiple-Function Variant for Multi-Variate Newton-Raphson Algorithm:

[1] **While** $(((\rho\text{-}\rho^*)/\rho > \epsilon)$ **OR** $((\rho_n\text{-}\rho_n^*)/\rho_n > \epsilon))$ {
[2]   **If** $((\rho\text{-}\rho^*)/\rho > \epsilon)$ {
[3] $a = a - (\rho^* - \rho)/\frac{\partial \rho}{\partial a}$
[4] $b = b - (\rho^* - \rho)/\frac{\partial \rho}{\partial b}$
[6] $\rho = a * A_n + b/S_n^2$ }
[7]   **If** $((\rho_n\text{-}\rho_n^*)/\rho_n > \epsilon)$ {
[8] $a = a - (\rho_n^* - \rho_n)/\frac{\partial \rho_n}{\partial a}$
[9] $b = b - (\rho_n^* - \rho_n)/\frac{\partial \rho_n}{\partial b}$
[10] $\rho_n = a * A_n + b/S_n^2$ }}

Parameter ρ_n refers to the correlation predicted for the nth design guarantee for the parameter a and b in the current iteration, whereas ρ_n^* indicates the correlation given by the nth design guarantee in the manual. Notice that in reality, the design guarantees do not directly give the correlation, but rather a resulting statistical parameter such as standard deviation of mismatch for that particular dimension and spacing. Hence, in each iteration of the algorithm, using the a and b of the current iteration, a Monte Carlo is run on the field solver and the resulting statistical parameter for mismatch is used to compare with the one given in the manual. As Newton-Raphson is known to be fast, convergence is achieved in few iterations depending on the accuracy level set by the parameter ϵ and a good initial guess.

The algorithm is given above for the case when there are two design rules given in the design manual. Each criterion corresponds to one particular area and spacing combination. By modifying this formulation, whether there are single or multiple matching criteria in the design manual, a model can be extracted. For the single-criterion case, the statements following the **OR** and the second **If** block can be eliminated. If there are more than two criteria, then, that many additional blocks are added **OR**-wise into the **while** statement and corresponding **If** clauses are added to the algorithm. The algorithm starts with the first design guarantee. If a and b provide a close estimation for the standard deviation of mismatch to the design manual, then the **while** statement moves to the next design guarantee and tries to optimize a and b for it, until the final a and b can satisfy the same ϵ for each of the design guarantees. To avoid becoming stuck at local minimum by optimizing exhaustively for a single function, a modified version may be considered, where instead of
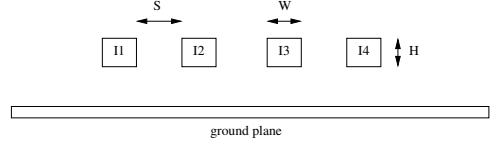

Figure 1: Matched interconnects over a ground plane

rolling back to the first design guarantee in each **while**, the least-used design guarantee is used in turn for optimization.

4.3 Correlation Model Decomposition for a Close Initial Guess

As the area of matched interconnects increases or the spacing decreases, the correlation increases linearly and quadratically, respectively. This analytic model has been proven to work well for small spacings. This restriction is justifiable as the spacing range as well as the area range will be restricted by the process. For example, assuming $0.12^2 < A < 0.36^2$ μm^2 and $0.12 < S < 0.36 \mu m$, the model can be decomposed to:

$$f = a' * A/0.36^2 + b' * 0.12^2/S^2 \qquad (5)$$

where the maximum area has been used for the first term and minimum spacing squared has been used for the second term as normalization numbers. Now, a' and b' indicate the effective area-dependence and spacing-dependence weights on the final correlation. For example, area-dependence could be more influential than the spacing dependence. If each part is equally important and the normalization constants are chosen according to the technology, a' and b' would be chosen as 0.5 each, hence making the sum equal to 1. A correlation of 1 is the maximum value which the correlation factor can take by definition. However, a correlation of value 1 would occur only if the two lines have the exact same variations, which is not realistic. In practice, a' and b' could add up to somewhere around 0.9. Furthermore, the constants chosen during the decomposition does not exactly correspond to the actual constants as the optimization step will help them converge to their actual values. Such a decomposition makes it possible to come up with close-to-real initial guesses for a and b, which will be helpful in the parameter extraction step that comes next.

5. GENERATION OF NEW GUARANTEES

Given a and b, more $A - S$ combinations can now be generated. Monte Carlo for field solutions on various $A - S$ combinations and interconnect patterns are run. Mismatch models are then extracted by regression on simulation data. To extract the mismatch, we propose to use separate Monte Carlo simulations for each area and length combination. For a single area and spacing, 100 to 1000 Monte Carlo simulations can be run. For each simulation, an interconnect pattern is selected and widths and heights of the interconnects are generated according to the correlation model and the extracted values of a and b.

5.1 The Choice of Mismatch Metric

In this work, we have considered two types of mismatch metrics. The percentage metric is calculated using the ra-

tio of standard deviation of the distribution for the difference of capacitances of interconnects 2 and 3, divided by the mean of the distribution for the capacitance of interconnect 2. We have used the following metric to fit a regression model which can directly predict the mismatch for each (A,S) combination.

$$mismatch\ metric = \frac{\sigma(mismatch\ of\ I2 - I3)}{\sigma(I2)} \quad (6)$$

Essentially in this metric, standard deviation of the difference of the middle-pair is divided by the standard deviation of one of the middle pair interconnects. It might be beneficial to normalize these metrics with area ratios.

5.2 Regression Model for Mismatch

A regression model similar to the proposed correlation model is used, with some modifications. A constant term is also added for better fit. A high correlation means a lower mismatch, hence A and S^2 have been inverted for the regression model:

$$mismatch = f(A, S) = (e + g/A + f * S^2) \quad (7)$$

Here, parameters e, g and f are fitting constants. We have provided this regression model to illustrate the methodology, but in reality a more accurate regression function should be chosen.

5.3 Handling Resistance Mismatch

Resistance mismatch does not require field solutions. While extracting the correlation model, each resistance for a particular pattern is calculated according to the following formula by perturbing each physical dimension:

$$R = \frac{\rho.L}{A} \quad (8)$$

Here, ρ is conductivity and assumed to be constant, and $A = W.H$. Then, the same mismatch metric is used separately on the resistance Monte-Carlo data, followed by a regression fit.

5.4 Consideration of Pattern Density

Design guarantees in the manuals bring on restrictions to the allowed minimum and maximum interconnect density due to the chemical-mechanical polishing step in the manufacturing process. We have considered these cases in our analysis. Maximum and minimum patterns, in a way, are like the worst-case points of a process. In the regression analysis, we have used these maximum and minimum points in order to fit the model, so that any valid (A,S) combination falls into this range.

5.5 Special Case: Edge Matching

Chemical-mechanical polishing requires dummy interconnects to avoid dishing and erosion. However, on certain designs, inclusion of dummy interconnects might not be possible due to reasons such as chip area. For example, a shape constraint can apply for a clock h-tree as in Figure 2. Trying to add grounded-dummy interconnects to an h-tree would result in contradictory placement of interconnect dummies for various levels of the clock tree as shown in Figure 3. As
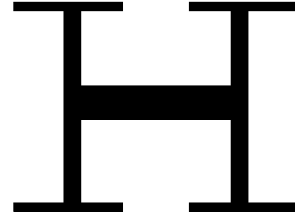

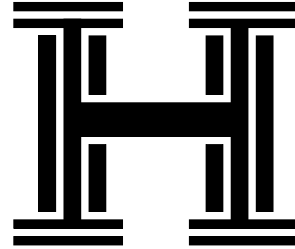**Figure 2: A representative h-tree**

Figure 3: Dummy insertion to the h-tree

certain lines are orthogonal, it may not be possible to accurately optimize regularity by adding regular ground-tied dummies. Also, dummies may need to be avoided due to other constraints such as coupling noise.

When dummy lines are not present, matching of a line at the edge and its neighbor will be different than the matching of two middle lines. For example, matching of $I1 - I2$ or $I3 - I4$ can be different than matching of $I2 - I3$. Edge matching can be handled as special cases if increased accuracy is needed. The standard deviation of matching for this case will have a bias (or rather, a non-zero mean in the density of mismatch), as the line at the edge lacks a coupling capacitor on one side. These conditions are handled by modeling the edge matching by a separate function.

6. EXPERIMENTAL RESULTS

Parameter values used in the experimentation are based on 45nm parameters. Minimum width and spacing used are 120nm. Height is also selected as 120nm and the dielectric constant is selected to be a constant of 3 all around the interconnects in the simulation box. Minimum pattern density is selected to be 25% and the maximum as 75%. Raphael from Synopsys is used for the field simulations. A standard deviation of 10% for process variations is assumed. We have assumed that total capacitance mismatch guarantee data is provided in the manual as the starting point.

The multi-function variant of the multi-variate Newton-Raphson algorithm initially had convergence problems. We have attributed the problem to large derivatives used while updating the parameters. Multiplying all the derivatives, $\frac{\partial \rho_n}{\partial a}$, etc., with a constant of 0.5 fixed the problem. Using the variables a and b as $0.45/(0.36*0.12)$ and $0.45*0.12*0.12$ and initializing them as $0.50/(2*0.12)$ and $0.50*0.01*0.01$ respectively, convergence is achieved in only 2 iterations for an error rate of 10E-4.

Using the extracted correlation parameters a and b, widths and heights of the transistors are assigned values using Equations in Section 4.2 for each Monte Carlo run. The histogram for the capacitance of interconnect 2 is acquired through
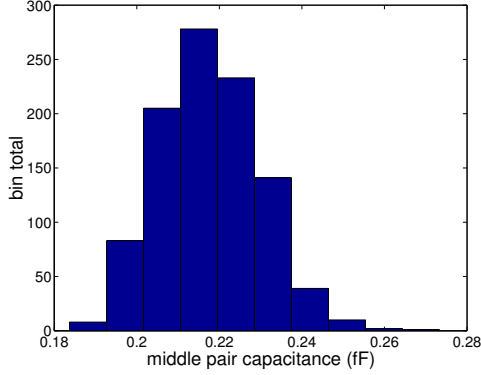
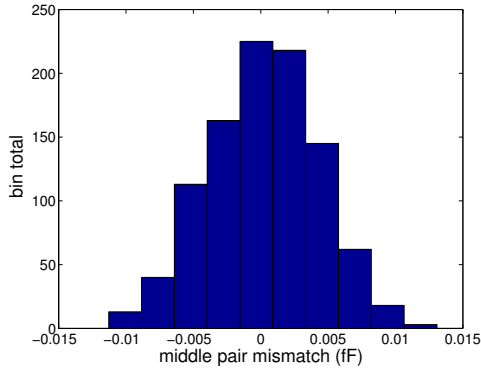**Figure 4: Histogram for density of capacitance for interconnect 2**

Figure 5: Histogram for density of mismatch between capacitances for interconnects 2 and 3 (middle pair)

Figure 6: Histogram for density of capacitance for interconnects 1 and 2 (edge pair)

Table 1: Percent Mismatch for High and Low Correlation

percent mismatch:	mid-pair	edge-pair
max density, $\rho =0$	5.44%	5.65%
max density, $\rho =0.9$	3.56%	5.67%
50% density, $\rho =0$	4.62%	4.28%
50% density, $\rho =0.9$	1.51%	1.42%

a correlation factor of 0 and 0.9. The experiments are done both for maximum density and 50% density. For the latter, both W and S are selected as 120nm or 360nm. The results are given in Table 1. The percentage mismatch definition is used for the table.

From the table, we can conclude that edge matching becomes an issue when pattern density is higher. This happens, as a higher pattern density means that coupling between interconnects is more. As one interconnect lacks a coupling on one side for edge-pair mismatch, as substantiated by the experimental results. Also, increasing the correlation results in less mismatch, as each parameter is closer in value to the one on the neighboring line.

Next, using the extracted a and b parameters, we have included process variations on both width and height dimensions. The results are summarized in Table 2 for maximum, minimum and 50% density conditions.

It can be concluded from the table that mismatch is more sensitive to the nominal value of the width for the assigned sizes. We have used a mismatch metric, where standard de-

1000 Monte Carlo runs as shown in Figure 4. The mismatch histogram is acquired by taking the difference of capacitances of interconnects 2 and 3 after the Monte Carlo runs as shown in Figure 5. The mean value is 0 as expected. For the edge matching, difference of capacitances between interconnects 1 and 2 is taken. This is shown in Figure 6, where a non-zero mean can be observed. This bias comes from the fact that interconnect-1 lacks one coupling capacitance on the outer side.

When only middle interconnects are assigned process variations, the mismatch is overestimated by 4.24% as compared to assigning process variations to all lines. As each line is correlated, the final capacitances of interconnects on the chip are closer to each other being on separate ends of the density tail, which would cause the unrealistic overestimation.

Maximum interconnect density is considered by assigning W as 360nm and S as 120nm, which corresponds to 75% density. For minimum density, W is assigned 120nm and S is assigned 360nm for 25% density.

The difference of middle-pair matching between using 4 and 10 total lines in the simulation window is evaluated to be less than 1%. Hence using 4 lines is sufficient and we do not have to consume extra simulation time.

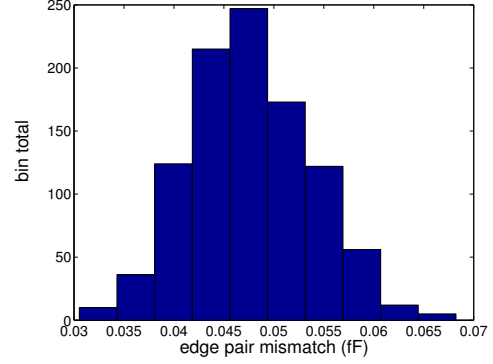Monte-Carlo analyses using process variations have been run for both middle-pair and edge-pair matching, both for

Table 2: Percent Mismatch for Various Densities

percent mismatch:	mid-pair	edge-pair
max density, $\rho =0$	5.44%	5.65%
max density, $\rho =$model	3.56%	5.67%
50% density, $\rho =0$,W=120nm	5.44%	5.65%
50% density, $\rho =$model,W=120nm	3.56%	5.67%
50% density, $\rho =0$,W=360nm	5.44%	5.65%
50% density, $\rho =$model,W=360nm	3.56%	5.67%
min density, $\rho =0$	4.62%	4.28%
min density, $\rho =0.9$	1.51%	1.42%

Table 3: Mismatch Using Proposed Metric

σ/σ mismatch:	mid-pair	edge-pair
max density, ρ =model	0.3655	0.5226
50% density, ρ =model,W=120nm	0.7409	0.7810
50% density, ρ =model,W=360nm	0.9079	0.8775
min density, ρ =model	0.8137	0.8249

viation of mismatch divided by the standard deviation of the distribution of the interconnect 2, as described previously. The results are presented in Table 3.

The regression model is fit on the data. The extracted parameters were 0.5298, 0.0392 and 1.1239 for e, f and g respectively. The regression model has shown an average error of 6.75%. Although this may be considered inaccurate to a degree, the purpose of this paper is not to propose a good regression model. It is given here only for illustrating the methodology.

Notice that edge matching becomes an issue for the maximum density case, where the coupling is most dominant, hence the variations in the coupling are able to affect the standard deviation ratios besides causing the constant bias. This situation can be handled by using a separate set of fitting constants e-f for the edge matching.

We have then used the mismatch model to fit a number of (A,S) combinations. Given such a combination, the end result is a guarantee of capacitance matching between two lines given in the form of a mismatch metric. For example, when interconnects of dimension $W = 240nm$ and $S = 240nm$ are evaluated both using simulation and through the regression model, the regression model was able to predict the capacitance matching guarantee with 4.15% accuracy as compared to the exact field simulation. This error is acceptable, considering the fact that the regression fit isn't perfect and can be improved through modifying Equation 7 and increasing the size of data used for regression. With this basic equation that we have used for demonstration, we were successful in implementing our design-guarantee generation methodology for interconnect matching.

7. CONCLUSIONS

New back-end rules are projected to provide matching guarantees for interconnects. To cover a continuous range of interconnect areas and spacings, which are not provided in the manual, we must generate guarantees from the provided ones. Direct extrapolation is not possible as the number of provided design guarantees is so limited; the given guarantees do not lend any way to account for edge matching; an extraction must be applied to acquire the process variations that have led to the guarantees given in the manual; and finally the standard capacitance-extraction procedure has to be modified to be able to account for mismatch. We have proposed a methodology that addresses the indicated issues. We have proposed a multi-function variant of Newton-Raphson for correlation extraction. We have introduced an initial point selection scheme to reduce the number of iterations in the algorithm while converging. A new mismatch metric is used. The methodology has been shown in an example using a basic regression model. The proposed method is also independent of the initial correlation model

assumption and the regression functions. This methodology will reduce design over-constraining and can be used in optimization tools, e.g. to optimize for interconnects.

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